Process of high power Schottky diodes on the AlGaN/GaN heterostructure epitaxied on Si
For my parents
For my brother
For Chahine and Eva
For abouna Michel
For Halim (rest in peace)
Thank you very much
Acknowledgment

This work was done in Laboratory GREMAN from the university of Tours under the supervision of Prof. Daniel Alquier.

First, I would like to thank Daniel Alquier and Marc Lethiecq for giving me the chance to work at GREMAN and accomplish my Master 2 internship and my thesis work at GREMAN.

During this period of time, Daniel was a very good advisor. He was always present when needed for scientific discussions, for thesis corrections and comments.

I thank Dr. Sylvie Contreras, Prof. Frederic Morancho, Dr. Yvon Cordier and Dr. Fabrizio Roccaforte for accepting to be members of the jury and for the time given to read and comment my manuscript.

Thanks to Frederic Cayrel, my second supervisor, for the advices, hints and corrections that gave me concerning my Ph.D. work and my teaching experience with him.

I owe him a very sincere thanks to Arnaud Yvon, engineer from STMicroelectronics, for all the time and advices he gave me. The motivation he gave me was a very important to achieve this Ph.D. work.

I am very thankful to my dear friend and colleague Rami Khazaka for all the fruitful discussions we had. The motivation he gave was one of a kind. I wish him all the luck.

I thank my friend Abhishek who was always here for me. An amazing person that gives and doesn’t expect back.

Thanks must also go to the GREMAN and STMicroelectronics staff who helped me with my work: the platform engineers, the CAD team, the Ph.D. students and the interns (Sebastien and Haoran) I worked with.

Finally, I express my deep gratitude to my family, parents Joseph and Jeanne d’ark, brother Michel “the yeti”, and uncles, Chahine, Michel and Halim. I owe them everything to their unconditional support and love in my life and education.
Abstract

Until now Silicon (Si) is the main material used in power conversion applications. These applications require low losses miniaturization and especially low-cost. Si-based devices are reaching their limits in this field. Wide band gap materials such as silicon carbide (SiC) and gallium nitride (GaN) started replacing Si. Nevertheless, despite the excellent properties and the devices performances already commercialized, SiC substrates are still too expensive. Thus, GaN has attracted researchers attention during the last decades. GaN is particularly interesting for power electronics. In addition to the high electron saturation velocity, GaN high breakdown electric field makes from this semiconductor the future of power devices, especially when epitaxied on low-cost substrates such as Si. Nowadays, the GaN epitaxy quality on large Si wafers is good enough to allow Schottky diodes development.

GREMAN laboratory, in collaboration with STMicroelectronics and many laboratories, has started developing Schottky diodes on GaN and AlGaN/GaN epitaxied on Si substrates.

In this work, we have developed Schottky diodes on the AlGaN/GaN heterostructure epitaxied on 8” Si substrates. A high density and mobility 2-dimensional electron gas, accumulating at the heterointerface, makes from the heterostructure an interesting solution for power devices. From the passivation layers and the recess to the metal contacts and the ion implantation, we have conducted the study on each technological step to process power diodes.

We have deposited silicon nitride (SiNx) passivations by plasma enhanced chemical vapor deposition (PECVD). We have found a nitrogen-rich SiNx layer with a very low tensile stress of 19 MPa. Atomic force microscopy (AFM) imaging have showed an invariant surface state and roughness of GaN before and after reactive ion etching of SiNx.

For the ohmic contact, we have focused on Au-free contacts such as titanium and aluminum. We have investigated the influence of the surface treatment, the annealing temperature and duration, the metal thickness and the AlGaN/GaN recess. The electrical results under the same process conditions were epitaxy-dependent. We have found a recess-free and Au-free contacts with a very low contact resistance (Rc) of 1 Ω.mm after annealing at 500 ºC, 3 min and 800 ºC, 30 s. The same contacts deposited on partial recessed heteroepitaxy have exhibited a 2.8 Ω.mm Rc with a sheet resistance of 480 Ω/sq.
Schottky to Schottky structures using 300 nm of Ni were fabricated and annealed at different temperatures and ambiances with different SiN$_x$ layers. On the recess-free heterostructure, the contacts annealed at 350 °C in N$_2$ have exhibited the lowest current densities of 1x10$^{-5}$ A.cm$^{-2}$. Energy-dispersive X-ray spectroscopy has showed a nitrogen-free Ni layer upon annealing at 350 °C while a N$_2$-rich layer was obtained after 550 °C annealing. On the other hand, the shallow recess exhibited the lowest leakage current density, using the SiN$_x$ passivation in tensile strain.

Then, these technological steps were combined during the process to form circular diodes on the AlGaN/GaN heterostructure. The ohmic contact and the passivation were fixed while the Schottky contact depth and annealing temperature were varied. The sample annealed at 400 °C with 30 nm of etching depth showed the most interesting results. A Schottky barrier height of 0.89 eV and an ideality factor of 1.49 were observed. These diodes also exhibited a very low leakage current density of 8.45x10$^{-8}$ A.mm$^{-1}$ before the diode breakdown which occurred between 480 V and 760 V.

Several issues in the process including the GaN temperature sensitivity and the p-type localized dopants activation are still to be overcome. High dose of implantation induces lattice disorder. Consequently, the lattice recovery, requiring high temperature treatment, can lead to efficient acceptor activation. We firstly have demonstrated the efficiency of a double cap layer, a magnetron sputtered crystalline aluminum nitride (AlN) layer and a PECVD SiO$_x$, after annealing at 1150 °C, 3 min. AFM images before and after the annealing have showed a similar surface. We have also showed the efficiency of a multi-temperature annealing (800 °C for 12 h and 1150 °C for 3 min) to partially recover the GaN lattice from the damages and to activate dopants. The X-ray diffraction have showed that the GaN (0002) satellite peak (related to ion implantation), disappears after annealing. Furthermore, photoluminescence has revealed a transition at 3.242 eV involving an Mg$_{Ga}$ shallow acceptor and a shallow donor.

We believe that our results are very promising in the power conversion field. The very low leakage current combined with a high barrier height present a solution for the high losses of the current power devices in the blocking mode without compromising the forward bias. The design and the devices reliability are the perspectives subject to further investigations.

Keywords: wide band gap, GaN, passivation, ohmic contact, Schottky contact, ion implantation, electrical characterization.
Résumé

Les exigences en termes de tenue inverse en tension, de fonctionnement à haute température et les problématiques d’économie d’énergie mettent en évidence les limites du silicium (Si) pour les composants de puissance. Les convertisseurs à base de Si atteignent leurs limites. Ces systèmes doivent présenter de faibles pertes énergétiques et surtout un faible coût, tout en conservant une dimension raisonnable. Face à ces besoins, le carbur de silicium (SiC) et le nitrure de gallium (GaN), semi-conducteurs dits à « grand gap » sont des candidats idéaux pour réaliser des redresseurs. Néanmoins, malgré les excellentes propriétés et performances des composants déjà commercialisés, les substrats SiC sont encore coûteux. Ainsi, le GaN, avec sa vitesse de saturation des électrons et son champ électrique de claquage élevés, a attiré l’attention des chercheurs au cours des dernières décennies. En effet, les progrès de l’épitaxie du GaN sur des substrats Si de large diamètre et à bas coût, ont permis d’envisager le développement de diodes Schottky sur GaN.

Le laboratoire GREMAN, en collaboration avec la société STMicroelectronics et de nombreux laboratoires dans le cadre de plusieurs projets nationaux (G2REC, Tours 2015), a commencé à développer des diodes Schottky sur GaN et sur l’hétérostructure AlGaN/GaN epitaxiées sur Si.

Dans le cadre de ce travail, il s’agit d’exploiter la propriété particulière de l’empilement AlGaN/GaN qui génère un gaz 2D d’électrons de densité et de mobilité très élevées. Nous avons développé des diodes Schottky sur l’AlGaN/GaN épitaxiée sur des substrats en Si 8”.

Nous avons étudié chaque étape technologique telles que les couches de passivation, la gravure, les contacts métalliques ainsi que l’implantation ionique pour atteindre notre objectif.

Nous avons déposé des passivations en nitrure de silicium (SiNx) par dépôt chimique en phase vapeur assisté par plasma (PECVD). Nous avons trouvé une couche de SiNx riche en azote en faible traction (19 MPa). En outre, L’imagerie par microscopie à force atomique (AFM) a montré l’efficacité de la gravure du SiNx par ion réactif.

Concernant le contact ohmique, nous nous sommes concentrés sur les contacts sans Au tels que le titane et l’aluminium. Nous avons étudié l’influence du traitement de surface, la température, la durée du recuit, l’épaisseur du métal ainsi que la gravure de l’AlGaN/GaN. Différentes épitaxies ont également fait l’objet d’études. Les mesures électriques ont montré une très faible résistance de contact (Rc) de 1 Ω.mm sur une hétérostructure sans gravure et un contact sans
Au recuit à 500 °C, 3 min et 800 °C, 30 s. Les échantillons avec une gravure partielle de l’AlGaN ont présenté une Rc de 2,8 Ω.mm avec une résistance $R_{sh}$ de 480 Ω carré.

Des structures tête-bêche avec 300 nm de Ni ont été fabriquées, recuites à différentes températures et en utilisant différentes couches de SiN. L’analyse dispersive en énergie n’a montré aucune trace d’azote après recuit à 350 °C tandis qu’une couche riche en N₂ a été mise en évidence après recuit à 550 °C. Néanmoins, l’échantillon gravé superficiellement et recuit à 350 °C a présenté une faible densité de courant de fuite à -200 V.

Ces étapes technologiques ont été combinées pour fabriquer des diodes Schottky. Le contact ohmique et la passivation ont été fixés tandis que nous avons fait varier la profondeur de contact Schottky et la température de recuit. L’échantillon recuit à 400 °C avec 30 nm de profondeur de gravure a montré les meilleurs résultats, notamment une hauteur de barrière de 0,89 eV et un facteur d’idéalité de 1,49. Ces diodes présentaient également une très faible densité de courant de fuite de $8.45 \times 10^{-8}$ A.mm⁻¹ à -400 V et une tension de claquage entre 480 V et 760 V.

Les verrous qui subsistent sont la sensibilité du GaN à la température et l’activation des dopants implantés. L’implantation ionique induit des défauts et leur guérison ainsi que l’activation des dopants doit passer par un traitement thermique. Il faut alors recourir à l’utilisation d’une couche de protection. Nous avons montré l’efficacité d’une double couche de protection, de nitrure d’aluminium cristallin obtenue par dépôt physique en phase vapeur et de SiOₓ déposé par PECVD, durant un recuit à 1150 ° C, 3 min. Les images AFM avant et après recuit ont montré une surface lisse de faible rugosité. Nous avons également montré l’efficacité d’un double recuit à 800 °C, 12 h et 1150 °C, 3 min pour réparer partiellement le réseau et activer les dopants. La diffraction des rayons-X a montré la disparition du pic lié à l’implantation, après ce recuit. En outre, la photoluminescence a révélé la présence d’un pic à 3,242 eV impliquant une transition entre accepteur (MgGa) et donneur peu profond.

Nos résultats sont prometteurs dans ce domaine d’application. Le très faible courant de fuite est ici combiné à une hauteur de barrière élevée. Cela présente une solution possible pour remplacer les composants de puissance actuels. Le design et la fiabilité font parties des perspectives à étudier prochainement.

Mots clés : grand gap, GaN, passivation, contact ohmique, contact Schottky, implantation ionique, caractérisation électrique.
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Introduction

Heading towards a future, as impressive as the technology is, electronic devices harmonized our life. One of the hidden side of the technology is the electrical power conversion. From smartphones to hybrid cars and planes, converting the electric power is achieved mainly by semiconductor devices also known as power devices. Reducing the switching losses results in a lower electricity consumption. Hence, efficient power devices with low switching losses help reducing the CO₂ emissions. In fact, the CO₂ emissions are threatening the entire globe as highlighted in the last climate change conference, COP21 which was held in Paris. Thus, limiting this gas emission lies within the objectives of both researchers and industrials at the international level.

To date, silicon (Si) remains the most used material in power conversion applications due to the features that this material can offer. In fact, many decades of research on Si led to a high purity and low cost material with large substrates diameter. Nevertheless, the theoretical limits imposed by the Si intrinsic properties meets with the desire to fabricate economic, reliable and highly efficient power devices. Seeking new solutions, the scientists have investigated wide band gap materials such as gallium nitride (GaN) and silicon carbide (SiC). The high electric field and the high electron saturation velocity are the main advantages of these materials compared to Si.

SiC power devices have been widely studied during the last decades and are now commercialized. However, despite the high quality homoepitaxial growth of SiC, the high cost and small diameters substrates result, for decades, in expensive devices. This trend may change due to the availability of 6 in. wafers at reasonable prices. In the meantime, the scientists started questing efficient, yet low cost power devices.

The first devices development on GaN were done in optoelectronics. In 1991, Nakamura et al. ¹ have published on the first “high-power p-n junction blue-light-emitting diodes (LEDs)” on GaN films grown with GaN buffer layers. They have reported an output power almost 10 times higher than that of conventional SiC blue LEDs. This direct band gap material is now one of the most used materials for white and blue optoelectronic LEDs or blue lasers. Last decades have brought commercial viability of GaN based photonic systems. Due to GaN properties mentioned previously, last decades have also evidenced an astonishing progress
of GaN-based field effect transistors. Now used to manufacture high electron mobility transistors (HEMTs), new perspectives are opened to GaN in power electronics. Among these applications, Schottky diode is one of the most expected devices. However, Schottky diode on GaN can be commercially viable only if researchers succeeded to reduce the final device cost. Hence, the epitaxial growth of GaN on large diameter Si substrates appears as the best approach to achieve this goal.

High breakdown voltage, fast switching and low leakage current Schottky diodes are used in power factor correctors (PFC). These Schottky diodes also called “boost” diodes are already commercialized by STMicroelectronics on SiC. However, the device cost is still relatively high. Reducing the diode cost can be achieved by processing it on GaN-on-Si. For this reason and as part of two French national projects (G2Rec and Tours2015), GREMAN laboratory, in collaboration with STMicroelectronics (Tours - France) and many laboratories, started developing, firstly, Schottky diodes on thick GaN-on-Si. Many PhDs were successfully conducted to achieve this goal. Nevertheless, technological challenges have to be overcome. Among them, doping by implantation (for p-type doping) and GaN etching (to reach n+ doped regions) remain the major obstacles to overcome. An alternative solution is to process the Schottky diode on AlGaN/GaN heterostructure epitaxied on Si. The heterostructure benefits from the polarizations induced in the layers without any additional doping. Under specific conditions (discussed in Chapter 1), a two-dimensional electron gas (2DEG) is confined at the AlGaN/GaN interface. The electron mobility and density are relatively high making the heterostructure a promising candidate for high power devices.

In order to shed more light on these issues, this manuscript aims to investigate the different technological steps to process high power diodes with breakdown voltages of 600 V and up to 1200 V in blocking mode. From the metal contacts (ohmic and Schottky) to the passivations and the ion implantation, the development of each step was conducted to reach our final goal.

Chapter 1 presents the III-N materials crystalline structures and the possible growth methods and substrate choice. The piezoelectric and spontaneous polarizations, responsible for the creation of the 2DEG at the heterointerface, are explained in details. HEMTs and Schottky diodes GaN-based applications are presented. Finally, an overview of the technological steps used to process Schottky diodes on the heterostructure and the literature comparison from each step is presented.
Chapter 2 shows a comparison between the different heterostructures provided by different suppliers. The studied technological steps are discussed. The silicon nitride (SiNx) passivation choice is presented in the second section of this chapter. The last two sections are dedicated with the Ohmic and Schottky contacts. A summary of the metal/semiconductor band theory and the carrier transport are presented. The influence of the Ohmic contact choice, the surface treatments, the annealing and the recess are presented in details with the corresponding electrical results. Various AlGaN/GaN heteroepitaxies are processed to obtain the lowest contact resistance. Schottky to Schottky structures were used to study the effect of the annealing, the recess and the passivation of the leakage current.

Chapter 3 regroups all the technological steps presented previously to process and characterize full Schottky diodes. The electrical parameters are extracted from the forward and reverse characteristics. The anneal temperature and the anode recess are varied to obtain the optimum barrier height, ideality factor, ON-state resistance and voltage and especially the leakage current and the breakdown voltage. A state of the art comparison and design optimization are also presented. A general conclusion summarizes the most relevant results of this manuscript and presents new perspectives following our work.

In the Chapter 4, ion implantation channeling and induced damages in GaN crystalline structure are addressed. GaN surface sensibility to high thermal treatments is elucidated with the importance of using cap-layers during high temperature annealings. The efficiency of the AlN/SiOx double cap-layer after thermal treatment and etching is presented. Very smooth GaN surface morphology is obtained after low and high temperature annealings (800 °C and 1150 °C, respectively). The double annealings effect on Mg-implanted GaN (GaN:Mg) protected by AlN/SiOx double cap-layer are presented. The crystalline, morphological and optical characterizations are highlighted. Finally, an attempt to activate the dopants by laser irradiation is discussed.
Chapter 1. AlGaN/GaN heterostructure properties and applications
In this chapter, we first discuss III-N materials structures and their possible growth methods as well as the substrate choice. Then, we explain both spontaneous and piezoelectric polarizations that result in the creation of the 2DEG at the heterointerface. We also present GaN-based applications, namely HEMTs and Schottky diodes on the heterostructure. Finally, we describe the technological steps used to process the Schottky diodes on such heterostructures.
1.1 III-N materials

1.1.1 Crystalline structure

The III-nitride materials, such as GaN, aluminum nitride (AlN) and indium nitride (InN), can be found in three different crystal structures: rock-salt, zinc-blende and wurtzite. The rock-salt structure can be obtained under high pressure conditions. Furthermore, rock-salt structure cannot be obtained by any epitaxial growth, hence, it is a non-compatible structure for industrial applications. The zinc-blende structure is formed by two face centered cubic crystals each composed of N or group III atoms and shifted of ¼ from the lattice diagonal. Under ambient conditions, wurtzite structure is the only thermodynamically stable phase. The hexagonal unit cell of the wurtzite structure leads to two lattice constants, a and c, as shown in Fig. 1-1a. It is formed by two interpenetrating hexagonal lattices, shifted by 3/8.c with respect to each other. Each hexagonal lattice is formed with one type of atom and each atom forms a tetrahedron bond with four atoms of different type (Fig. 1-1b). Due to the wide variation in electronegativity of Ga and N atoms in wurtzite GaN crystal, the chemical bonds are ionic. In addition, GaN is non-symmetric along the c-axis ([0001] direction). Consequently, [0001] and [000̅1] directions are not equivalent. Thus, two different faces of GaN can be defined. These different faces, presented in Fig. 1-2, are known as Ga or N-face, that corresponds, respectively, to [0001] and [000̅1] directions. It is important to distinct these two polarities that can be obtained in special growth conditions. The properties of wurtzite GaN depend on the structure polarity. High surface roughness is the major inconvenient of N-face, while Ga-face benefits from a smooth surface which is more suitable for the devices we aim to develop (electronic devices). III-N materials can also form ternary alloys such as Al$_x$Ga$_{1-x}$N, In$_x$Al$_{1-x}$N and also In$_x$Ga$_{1-x}$N, where $x$ represents the material composition. The epitaxy of the III-N materials and the substrate choice will be presented in the following section.
Fig. 1-1. (a) Hexagonal (wurtzite) lattice structure of c-axis III-N, (b) tetrahedron bonding of each atom with four atoms of different type.

Fig. 1-2. Crystallographic orientation [0001] and [0001] as a function of gallium and nitrogen polarity.

1.1.2 GaN epitaxy and the choice of the substrate

The epitaxy of GaN-based heterostructures can be achieved by different techniques. We can mention the molecular beam epitaxy (MBE), hybrid vapor phase epitaxy (HVPE) and metal-organic chemical vapor deposition (MOCVD). To avoid long-drawn-out text, the MBE and HVPE techniques, that were not used in this work, are explained elsewhere and we will focus on MOCVD deposition technique that is also the most used technique in industrial semiconductor growth for device fabrication (HEMTs, LEDs, laser). This technique uses metal-organic compounds such as Trimethylgallium (TMGa) or Trimethylaluminium (TMAI) as precursors of Ga for GaN and Al for AlN epitaxies. A carrier gas such as hydrogen (H₂) or nitrogen (N₂) is used to transfer TMGa and TMAI to the heated substrate. Ammonia (NH₃) is
used as precursor for nitrogen. This growth technique enables high rate epitaxy on large diameter substrates (6 and 8 in.) and good crystalline quality. During the epitaxy, the substrate is heated between 1000 °C and 1100 °C. The mean free path of the atoms on the surface is increased, which results in a good crystalline quality and a low-density epi-layers. The substrate choice also plays an important role in the epitaxy. Bulk GaN substrate with low dislocation density is the best solution for GaN epitaxy leading to a homoepitaxy. The homoepitaxy results in low dislocations GaN epi-layers very suitable for power applications (the purpose of our study). Unfortunately, bulk GaN substrates are difficult to obtain due to the extreme growth conditions (2220 °C and 6 GPa) resulting in expensive GaN substrates with small dimensions, unsuitable for microelectronics industry. Another solution to face these difficulties is the heteroepitaxy of GaN meaning a growth on a “foreign” substrate. The most used substrates for GaN growth are sapphire (Al₂O₃), SiC and Si. Table 1-1 shows these most used substrates for wurtzite GaN growth with some of their properties and some growth characteristics.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Crystalline structure</th>
<th>Lattice mismatch with GaN</th>
<th>Thermal expansion coefficients¹ (10⁻⁶ K⁻¹) at 300 K</th>
<th>Wafer size and Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>Hexagonal</td>
<td>0</td>
<td>5.59</td>
<td>2 - 4 in. Extremely high</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>Hexagonal</td>
<td>16% (30 ° rotation)²</td>
<td>7.5</td>
<td>2 – 8 in. Medium</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>Hexagonal</td>
<td>3.36%</td>
<td>4.2</td>
<td>2 – 8 in. Very high</td>
</tr>
<tr>
<td>Si (111)</td>
<td>Cubic</td>
<td>17%</td>
<td>2.6</td>
<td>2 – 12 in. low</td>
</tr>
</tbody>
</table>

Table 1-1. Most used substrates for wurtzite GaN growth.

GaN on Sapphire is widely used in optoelectronics applications. Although the huge lattice mismatch between both materials and the bad thermal conductivity of Sapphire (0.3 W.cm⁻¹.K⁻¹), this substrate is transparent in the visible wave length and has an excellent thermal stability.

GaN on SiC is used in applications for high-frequency where the thermal conditions are severe. The excellent thermal conductivity of SiC (4.5 W.cm⁻¹.K⁻¹) and the low lattice mismatch

¹ Volume variation related to temperature or pressure variation.
² GaN lattice 30° rotation to reduce lattice mismatch from initially 30% to 16%.
between GaN and SiC (3.5%) make the SiC substrate a good candidate for the epitaxy. However, SiC and Al₂O₃ substrates are much more expensive than Si ones. Furthermore, Si is available on larger diameters (up to 12 in.). In fact, the market demands low cost components with excellent properties. GaN epitaxy on Si can meet the requirements for low cost substrate and a possible integration of high power electronic devices on GaN with the Si-based ones.

Having said that, the thermal and lattice mismatches between GaN and Si have to be reduced in order to obtain low dislocation density and crack-free epi-layers. To face these problems, the presence of a buffer layer between the Si substrate and GaN/AlGaN epi-layers is mandatory. The buffer is, in fact, a stack of numerous layers that are binary or ternary III-N materials with high quality epitaxy (low dislocation density and low surface roughness). The presence of a buffer layer reduces considerably the strain in the GaN epi-layer. However, the buffer layer does not totally reduce the lattice mismatch, consequently, the dislocation density in the GaN epi-layer is higher than 10⁸ cm⁻². Furthermore, the buffer layer is considered as highly resistive since AlN layers (6.2 eV band gap at room temperature) are present in the stack. Consequently, the process of vertical components is complicated. Up to now, GaN is grown on 6 and 8 in. Si (111) substrates. In this work, an AlGaN/GaN heterostructure is epitaxied on 6 and 8 in. Si (111) substrates by MOCVD. The details of the epi-layers are given in Chapter 2. In the following section, we will see the properties of the AlGaN/GaN heterostructure. The spontaneous and piezoelectric polarizations will be presented.

1.2 AlGaN alloy: spontaneous and piezoelectric polarizations

1.2.1 Spontaneous polarization

As previously mentioned, GaN is non-symmetric along the c-axis. In addition, nitrogen ionicity is high. Both properties, together, lead to a polarization along the c-axis. Consequently, electric dipoles appear. Positive and negative charges are compensated in all the crystal. When charges are no longer compensated (due to surfaces/interfaces), it results in a two charge sheets with opposite signs at the interfaces, as represented in Fig. 1-3. This polarization is called spontaneous (Psp) since it occurs at equilibrium independently of the stress.
Table 1-2 shows the spontaneous polarization and the lattice parameters of the main III-Nitride materials.

<table>
<thead>
<tr>
<th>Wurtzite</th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>a (Å)</td>
<td>3.112</td>
<td>3.189</td>
<td>3.545</td>
</tr>
<tr>
<td>c (Å)</td>
<td>4.982</td>
<td>5.185</td>
<td>5.703</td>
</tr>
<tr>
<td>Psp (C.m$^{-2}$)</td>
<td>-0.081</td>
<td>-0.029</td>
<td>-0.032</td>
</tr>
</tbody>
</table>

According to Vegard’s law, the lattice parameters (a and c) of a ternary III-N alloy (A$_x$B$_{1-x}$N) can be calculated as follows:

$$a_{A_xB_{1-x}N}(x) = a_{AN}x + (1 - x)a_{BN}$$  \hspace{1cm} Eq. 1.1

$$c_{A_xB_{1-x}N}(x) = c_{AN}x + (1 - x)c_{BN}$$  \hspace{1cm} Eq. 1.2

Consequently, the spontaneous polarization in A$_x$B$_{1-x}$N is also calculated as follows:

$$P_{sp,A_xB_{1-x}N}(x) = P_{sp,AN}x + (1 - x)P_{sp,BN}$$  \hspace{1cm} Eq. 1.3

Thus, the spontaneous polarization in Al$_x$Ga$_{1-x}$N is obtained from the $P_{sp}$ of GaN, AlN and x, the composition of Aluminum (Al) in AlGaN. This results in:

$$P_{sp,Al_xGa_{1-x}N}(x) = -0.052x - 0.029 \text{ C.m}^{-2}$$  \hspace{1cm} Eq. 1.4

Spontaneous polarization in wurtzite III-N as a function of lattice parameter c is represented in Fig. 1-4.
Fig. 1-4 also shows that spontaneous polarization in GaN is constantly lower than the one in Al$_x$Ga$_{1-x}$N materials.

### 1.2.2 Piezoelectric polarization

Naturally, as showed in Table 1-2, a lattice mismatch exists between GaN and AlGaN. At the equilibrium, when a thin Al$_x$Ga$_{1-x}$N layer is grown on a thick GaN one, Al$_x$Ga$_{1-x}$N layer undergoes a strain related to lattice mismatch with GaN. As mentioned before, the growth direction is parallel to [0001] direction or $c$-axis. As a result, Al$_x$Ga$_{1-x}$N undertakes a biaxial expansion in plane and is grown on GaN with a tensile strain, as shown in Fig. 1-5a. This induce a polarization, called strain-induced or piezoelectric polarization ($P_{pe}$) that is calculated as follows:

$$P_{pe} = e_{33} \cdot \varepsilon_z + e_{31} \cdot (\varepsilon_x + \varepsilon_y)$$

Eq. 1.5

where $\varepsilon_x$, $\varepsilon_y$ and $\varepsilon_z$ are the in-plane and along $c$-axis ($\varepsilon_z$) strain, respectively, and $e_{33}$ and $e_{31}$ are the piezoelectric coefficients.
The strain in x and y directions is the same due to the six-fold rotational symmetry of wurtzite structures along the c-axis. Thus, the in-plane strain can be expressed:

\[ \varepsilon_x = \frac{(a-a_0)}{a_0} \quad \text{Eq. 1.6} \]

where \(a\) and \(a_0\), here, are the lattice constants of a strained (AlGaN) and an unstrained (relaxed GaN) layers, respectively, due to the large difference in the thickness of GaN and AlGaN layers.

The strain along the c-axis can be expressed similarly:

\[ \varepsilon_z = \frac{(c-c_0)}{c_0} \quad \text{Eq. 1.7} \]

where \(c\) and \(c_0\) are the lattice constants of a strained and an unstrained layers, respectively. The strain along c-axis and in-plane are correlated by the equation 1.8:

\[ \varepsilon_z = -2 \frac{C_{13}}{C_{33}} \varepsilon_x \quad \text{Eq. 1.8} \]

where \(C_{13}\) and \(C_{33}\) are the elastic constants of the layer. Combining equations 1.5, 1.6 and 1.8 leads to the following equation:

\[ P_{pe} = 2 \cdot \frac{(a-a_0)}{a_0} \left( e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right) \quad \text{Eq. 1.9} \]

Table 1-3. Lattice, elastic, piezoelectric constants and spontaneous polarization in III-Nitrides.

| Wurtzite       | AlN | GaN | InN  | AlxGa1-xN |  \\
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) (Å)</td>
<td>3.112</td>
<td>3.189</td>
<td>3.545</td>
<td>(a(x) = -0.077x + 3.189)</td>
<td>Eq. 1.10</td>
</tr>
<tr>
<td>(c) (Å)</td>
<td>4.982</td>
<td>5.185</td>
<td>5.703</td>
<td>(c(x) = -0.203x + 5.185)</td>
<td>Eq. 1.11</td>
</tr>
<tr>
<td>(P_{sp}) (C.m(^{-2}))</td>
<td>-0.081</td>
<td>-0.029</td>
<td>-0.032</td>
<td>(P_{sp}(x) = -0.052x - 0.029)</td>
<td>Eq. 1.4</td>
</tr>
<tr>
<td>(e_{33}) (C.m(^{-2}))</td>
<td>1.46 (^6)</td>
<td>0.73 (^6)</td>
<td>0.97 (^6)</td>
<td>(e_{33}(x) = 0.73x + 0.73)</td>
<td>Eq. 1.12</td>
</tr>
<tr>
<td>(e_{31}) (C.m(^{-2}))</td>
<td>-0.60 (^6)</td>
<td>-0.49 (^6)</td>
<td>-0.57 (^6)</td>
<td>(e_{31}(x) = -0.11x - 0.49)</td>
<td>Eq. 1.13</td>
</tr>
<tr>
<td>(C_{13}) (GPa)</td>
<td>108</td>
<td>103</td>
<td>92</td>
<td>(C_{13}(x) = 5x + 103)</td>
<td>Eq. 1.14</td>
</tr>
<tr>
<td>(C_{33}) (GPa)</td>
<td>373</td>
<td>405</td>
<td>224</td>
<td>(C_{33}(x) = -32x + 405)</td>
<td>Eq. 1.15</td>
</tr>
</tbody>
</table>

Table 1-3 shows the values of the lattice, elastic and piezoelectric constants and the spontaneous polarization in AlN, GaN, InN and their values as a function of x, Al composition, in Al\(_{x}\)Ga\(_{1-x}\)N. The equation function of x were calculated based on the values from Ref. \(^6\).

Since \(e_{31}\) is always negative, \(e_{33}\), \(C_{13}\) and \(C_{33}\) are always positive in all the III-Ns employed in electronic devices and \([e_{31} - e_{33} \frac{C_{13}}{C_{33}}]\) is negative, the piezoelectric polarization sign (negative or positive) will depend on \(\varepsilon_x\). \(P_{pe}\) is negative for tensile and positive for compressive strained...
layers, respectively. The spontaneous polarization of Ga(Al)-face in GaN/AlN heterostructures is always negative and pointing towards the substrate (Fig. 1-5b). Thus, in our case, a thin Al,Ga_{1-x}N layer (strained), epitaxied on a thick GaN layer (relaxed), results in a Ga(Al)-face heterostructure. This heterostructure is under tensile strain since $\varepsilon_x$ is always negative ($a_{\text{GaN}} > a_{\text{AlGaN}}$) resulting in a negative piezoelectric polarization parallel to the spontaneous one (pointing towards the substrate) (Fig. 1-5b). When increasing $x$, the lattice constant decreases and $[e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}}]$ increases (in absolute value) leading to an increase of the piezoelectric polarization (in absolute value) in AlGaN layer. In our case, for a Ga(Al)-face AlGaN on top of a thick GaN heterostructure, the GaN piezoelectric polarization is assumed close to zero.

As discussed before and shown in Fig. 1-5b, the spontaneous and piezoelectric polarization in AlGaN are negative and pointing towards the substrate. Fig. 1-6 shows the spontaneous, piezoelectric and the total polarizations in AlGaN layer as a function of the Al composition. The more the AlGaN layer is richer in Al, the higher the total polarization in AlGaN.

![Fig. 1-6. Calculated polarizations in AlGaN layer as a function of Al composition.](image)

Thus, at an abrupt interface of an AlGaN/GaN layer heterostructure, the polarization in the bilayer can increase or decrease, causing a polarization sheet charge density ($\sigma^{+}_{\text{pol}}$) that can be defined by:

$$\sigma^{+}_{\text{pol}} = P_{\text{AlGaN}} - P_{\text{GaN}} = [P_{\text{sp,AlGaN}} + P_{\text{pe,AlGaN}}] - P_{\text{sp, GaN}}$$

Eq. 1.16

The epitaxy, in our case, results in a Ga(Al)-face AlGaN on top of thick GaN heterostructure. Thus, the positive polarization-induced charge will be located at the AlGaN/GAN interface.
while the negative charge will be at the top of AlGaN layer (Fig. 1-5-b). Based on Table 1-3 and the equations reported above, the polarization-induced sheet charge density is positive. As a consequence of the increase in the polarization with the Al composition in AlGaN, the polarization-induced sheet charge density also increases as shown in Fig. 1-7. In the next paragraph, we will then see how it induces an electron gas.

![Graph](image)

**Fig. 1-7.** Calculated polarization sheet charge density caused by spontaneous and piezoelectric polarization at the interface of AlGaN/GaN heterostructure as a function of the composition of Al.

### 1.2.3 2DEG formation mechanism: the influence of $t_{\text{AlGaN}}$ and $x_{\text{AlGaN}}$

As mentioned previously, the polarization sheet charge density is positive in the case of Ga(Al)-face AlGaN/GaN. If the interface roughness is low enough and if the AlGaN/GaN band offset is reasonably high, free electrons will tend to compensate the positive polarization-induced charge at the interface, forming a 2DEG with a sheet concentration $n_s$. In the heterostructure, the AlGaN layer is called “barrier” and the GaN layer where the 2DEG is confined is called “channel”. As both layers are unintentionally doped, the origin of the 2DEG was still unclear. Smorchkova *et al.* 10 suggested, for the first time in 1999, the following theory: the origin of the 2DEG and the positive charge compensating the negative polarization-induced charge at top of the barrier layer is surface donor-like states, with an energy $E_D$ (Fig. 1-8a), located quite deep in the AlGaN band gap. When the barrier layer thickness is inferior to the critical thickness $t_{CR}$ (calculated later on), these donor states are occupied. Consequently, no 2DEG is confined at the interface, as shown in Fig. 1-8a. The donor-like are neutral when occupied ($t_{\text{AlGaN}}$ lower $t_{CR}$) and positive when emptied ($t_{\text{AlGaN}}$ higher $t_{CR}$). Once the barrier layer
thickness is higher than \( t_{CR} \), the Fermi level slides down to the donor-like level (Fig. 1-8b) and the electrons are then able to transfer from their occupied states to the empty conduction band forming a two-dimensional electron gas at the interface and leaving behind positive surface charge. The 2DEG is formed at 5 to 10 nm in the GaN layer at the interface with AlGaN. The 2DEG density increases as \( t_{AlGaN} \) is increased further. For \( t_{AlGaN} \gg t_{CR} \) and also assuming that the barrier does not reach another critical thickness at which relaxation occurs, the 2DEG density will keep increasing until it saturates at the value of the polarization-induced charge (Fig. 1-10).

For AlGaN thickness higher than \( t_{CR} \), 2DEG accumulates at the interface of the heterostructure. The sheet carrier density at the interface as a function of the Al composition is expected to be:

\[
\begin{align*}
n_s(x) &= \frac{\sigma_{Pol}(x) \cdot \varepsilon_0 \cdot \varepsilon(x)}{q} \left( q \Phi_b(x) + E_F(x) - \Delta E_C(x) \right) \\
    &= \text{Eq. 1.17}
\end{align*}
\]

where \( q \Phi_b \) is the barrier height of the contact, \( E_F \) Fermi level related to GaN conduction band edge, \( \Delta E_C \) is the conduction band offset between AlGaN and GaN at the interface, \( \varepsilon(x) \) is the \( Al_xGa_{1-x}N \) dielectric constant and \( t_{AlGaN} \) is the thickness of the \( Al_xGa_{1-x}N \) barrier. In order to determine the sheet carrier density as a function of \( x \) and the other parameters, some approximation are used as:

![Schematic band diagram of the surface donor-like model showing the evolution of the band structure in AlGaN/GaN heterostructure: with AlGaN thickness (a) lower and (b) higher than \( t_{CR} \).](image-url)
- dielectric constant:
  \[ \varepsilon(x) = -0.5x + 9.5 \]  
  Eq. 1.18

- Schottky barrier:
  \[ q\Phi_b(x) = (1.3x + 0.84) \text{ eV} \]  
  Eq. 1.19

- conduction band offset:
  \[ \Delta E_C(x) = 0.7[E_g(x) - E_g(0)] \]  
  Eq. 1.20

where \( E_g(x) \) is the band gap of AlGaN barrier:

\[
E_g(x) = xE_g(AlN) + (1 - x)E_g(GaN) - x(1 - x)1.0 \text{ eV}
\]
  Eq. 1.21

Since the Fermi level remains at the donor-like energy until all surface states are empty, we can neglect the width of the Fermi distribution and the Fermi level rise in the channel. The critical barrier thickness \( t_{CR} \) can hence be calculated as followed:

\[
t_{CR}(x) = (E_D(x) - \Delta E_C(x)). \frac{\varepsilon(x)}{q\sigma_{pol}(x)}
\]
  Eq. 1.22

Consequently, the 2DEG density as a function of \( t_{CR} \) is given by:

\[
q_n(x) = \sigma_{pol}(x)(1 - \frac{t_{CR}(x)}{t_{barrier}})
\]
  Eq. 1.23

![Critical thickness of the barrier as a function of Al composition calculated using eq. 1.22.](image)

Theoretical critical thickness of the barrier as a function of Al composition is presented in Fig. 1-9, showing the rapid decrease in \( t_{CR} \) when increasing the Al composition.

Fig. 1-10 shows the 2DEG density as a function of the barrier thickness for different Al concentrations. One can see that the 2DEG density rapidly increases when the barrier thickness exceeds \( t_{CR} \) then approaches the saturation value of \( \frac{\sigma_{pol}}{q} \) for \( t_{AlGaN} >> t_{CR} \). It is worth to mention that the positive polarization charge at AlGaN/GaN interface is not directly responsible for the
2DEG. The eq. 1.17 is a result of a complex energy distribution of surface states and leads to a \( t_{\text{AlGaN}} \) and \( x_{\text{Al}} \) dependence on \( n_s \). However, the result remains the same: the energy level between the Fermi level, the GaN conduction band edge and the occupied levels at the surface decreases when increasing the barrier thickness leading to the accumulation of the electrons at the interface (forming the 2DEG) with a density \( n_s \).

![2DEG density vs barrier thickness and Al composition](image)

**Fig. 1-10.** 2DEG density (full color) and \( \sigma_{\text{Pol}}/q \) (dotted line) as a function of the barrier thickness and barrier Al composition. Surface donor-like state model is used to calculate 2DEG density. (Eq. 1.23)

As mentioned before, for a fixed barrier thickness higher than \( t_{\text{CR}} \), \( n_s \) depends on \( x_{\text{Al}} \). However, an Al composition above 40% does not result in better device performances. In a matter of fact, for \( x_{\text{Al}} > 40\% \), the lattice and thermal mismatches between the barrier and the channel is high enough to cause a rough interface and high density structural defects in the barrier layer.

Ambacher *et al.* \(^5\) have reported a comparison of the calculated sheet carrier densities versus Al-content (for a 30 nm barrier layer) with sheet carrier concentrations experimentally determined by C-V and hall measurements. They have found a good agreement of the calculated and measured sheet carrier concentrations of the heterostructures when \( x_{\text{Al}} \) is between 15\% and 30\%. In our study, depending on the epitaxy and on the suppliers, 4 different Al compositions between 21.5\% and 26\% are used. The AlGaN barrier thickness varies between 18 nm and 29 nm. The suppliers’ epitaxy characterizations are reported in Chapter 2.
2DEG mobility

Another important parameter for the 2DEG is the electron mobility ($\mu_e$). If $n_s$ depends only on the Al composition and the thickness of the barrier, the electron mobility depends on the elastic and inelastic scattering mechanism of the carriers: ionized impurities, threading dislocations, interface roughness, alloy disorder, acoustic and optic phonons.

The impact on the mobility can be described as follows:

- The ionized impurities scattering has a weak impact on $\mu_e$ since their presence at the surface or in the barrier are spatially separated from the 2DEG.
- The threading dislocations act as acceptors-like defects, capturing electrons from conduction band, and are negatively charged. Consequently, a space charge region is formed around the dislocations. These dislocations, perpendicular to the 2DEG, results in the decrease in the 2DEG mobility.
- The interface roughness plays an important role when $n_s$ is high. When $n_s$ increases, the electrons are driven closer to the interface channel/barrier. Consequently, if the interface is rough, the electron mobility decreases.
- The alloy composition disorder in the barrier disturbs the periodicity of the potential well since a part of the 2DEG will get into the barrier. Alloy disorder can be seen as an electrical interface roughness rather than a geometric one. This scattering can be neglected by the insertion of a thin AlN layer between the channel and the barrier $^{11,12}$. Smorchkova et al. $^{11}$ have reported the enhancement of low-temperature electron mobility in AlN/GaN heterostructure in comparison to AlGaN/GaN heterostructure with similar 2DEG sheet density. They have suggested that the dominant scattering mechanisms limiting the electron mobility are alloy disorder and interface roughness scattering since the alloy disorder in binary compounds (AlN/GaN heterostructure) is negligible. They have also reported the improvement of the electron mobility in AlGaN/GaN heterostructure (especially at low temperature) by inserting 10 Å of AlN between AlGaN and GaN, thus, eliminating the alloy scattering of the 2DEG.
- The temperature dependent atom vibration releases a quantum of energy called “phonon”. The acoustic and optic phonons are also responsible of lowering the electron mobility at low and high temperatures, respectively $^{13}$.

Fig. 1-11 shows mobility as a function of temperature with a 2DEG density around $10^{13}$ cm$^{-2}$. 

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Fig. 1-11. Mobility as a function of temperature with a 2DEG density around $10^{13}$ cm$^{-2}$. The solid line represents the resulting mobility from all three scattering contributions. The piezoelectric scattering is small compared to the other two scattering processes. Until now, we saw the advantages of AlGaN/GaN heterostructure on GaN (bulk or epitaxy) or SiC. The electron mobility of GaN or SiC at room temperature (RT) is relatively low ($\sim$1000 cm$^2$.V$^{-1}$.s$^{-1}$ and 400 cm$^2$.V$^{-1}$.s$^{-1}$, respectively). However, the ability of the AlGaN/GaN heterostructure to create a 2DEG at the interface with high electron density ($\sim$1x10$^{13}$ cm$^{-2}$) and mobility ($>1500$ cm$^2$.V$^{-1}$.s$^{-1}$ at RT) compared to the value of GaN or SiC is one of the most important properties of III-N. In the next section, applications based on the heterostructure, such as HEMTs or Schottky diodes, are presented.

1.3 GaN-based Applications

As previously seen, the researchers were attracted by III-N alloys due to its direct band gap. III-N materials were used for novel optoelectronic devices such as blue and green LEDs$^{15,16}$ and laser diodes$^{17}$. Due to its wide band gap (3.4 eV), high breakdown field (330 V.$\mu$m$^{-1}$) and high saturation drift velocity ($2.5\times10^7$ cm.s$^{-1}$), GaN is now also used in electronic devices with applications in high speed and high power domains. In addition, excellent electronic transport properties have been achieved in III-N heterostructures using the piezoelectric enhancement mechanism. Owing to these properties, GaN-based devices are in the course of expansion. HEMTs and Schottky diodes are under intense worldwide research. In this part, we explain briefly the structure and the aim of these devices.
1.3.1 HEMTs

HEMTs also called TEGFETs (two-dimensional electron gas field effect transistors), represented in Fig. 1-12a, does not need any dopant incorporation (that limits the electron mobility in the channel) which is basically the main advantage of the structure.

Fig. 1-12. (a) Cross sectional view of an AlGaN/GaN HEMT and (b) band diagram showing the barrier height, the fermi level and the conduction band.

The gate contact is a Schottky contact. When applying a voltage at the gate, the 2DEG is modulated and modifies the current between the source and the drain $I_{DS}$. The energetic positions of the conduction and Fermi bands under the gate (Fig. 1-12b) are affected by the bias applied between the source and the gate $V_{GS}$. At $V_{GS} = 0$ V, AlGaN/GaN HEMTs are mainly normally-on. A negative $V_{GS}$ has to be applied to deplete the channel and block the current.

However, to reduce circuit complexity and power consumption, normally-off transistors are highly desirable for high voltage power switching applications. Several structures are proposed in the literature to obtain normally-off HEMTs.

The main structures are:

- Gate recess structure

The gate recess brings the gate closer to the AlGaN/GaN interface (Fig. 1-13a) and the threshold voltage increases. The Schottky contact creates a depletion region that reaches the AlGaN/GaN interface and depletes the channel. Consequently, the gate recess structure results in a normally-off HEMTs 18.
- Thin AlGaN barrier layer

Equivalently to the gate recess structure, the thin barrier layer structure brings the Schottky contact closer to the AlGaN/GaN interface (Fig. 1-13b). However, the Al composition is increased to compensate the 2DEG density resulting from the thin AlGaN barrier 19.

- Fluorine plasma treatment or ion implantation

Considering the low thickness if the AlGaN barrier (between 15 and 35 nm), a fluorine plasma treatment or ion implantation is a process that enables the modulation of the channel threshold voltage. The presence of negative fluorine ions causes the lift of the potential well at the AlGaN/GaN interface above the Fermi level. However, the main inconvenient of this technique is the penetration of the fluorine ions in the channel degrading the 2DEG mobility 20,21. Fig. 1-13c shows a cross section view of the normally-off HEMT after fluorine ion implantation.

- P-GaN gate HEMT

In this type of structure, a polarization discontinuity is created between the barrier and the p-GaN resulting in a negative charge at the p-GaN/AlGaN interface (Fig. 1-13d). Consequently, the potential well at the AlGaN/GaN interface is lifted up.

- P-AlGaN gate injection structure

The p-GaN of the previous structure is replaced by a p-AlGaN layer (Fig. 1-13e). The Fermi level shifts towards the valence band in the p-AlGaN layer resulting in the shift of the conduction band at the equilibrium. When using highly doped p-AlGaN layer, the potential well at the AlGaN/GaN interface is elevated above the Fermi level achieving the normally-off operation.
Fig. 1-13. Schematic cross section of the normally-off structures using (a) gate recess, (b) thin AlGaN, (c) fluorine incorporation, (d) p-GaN, (e) p-AlGaN gates and (f) InGaN cap-layer, respectively.

- InGaN cap-layer structure

This approach consists in employing the polarization-induced field in the InGaN cap and the negative charge in the p-InGaN. Consequently, the conduction band in the AlGaN barrier is raised and the HEMT operates in normally-off mode \(^{22,23}\).

Mizutani et al. \(^{23}\) have reported on normally-off HEMT using i-InGaN (Fig. 1-13f) and p-InGaN on top of the barrier. They have reported an upward shift of the conduction band due to presence of InGaN (Fig. 1-14b). Further conduction band shift occurs when using p-InGaN (Fig. 1-14c). They have also reported the increase of the threshold voltage from -1 to 0.2 and 1.2 V, for the AlGaN/GaN HEMTs without an InGaN cap, with an i-InGaN cap, and with a p-InGaN cap, respectively as shown in Fig. 1-14d.
The HEMTs work at high frequencies and consequently are mostly used in the communications (due to the high carrier mobility). AlGaN/GaN HEMTs show faster switching and low losses comparing to transistors on Si, GaAs or SiGe.

### 1.3.2 Schottky diodes

To achieve these diodes, several technological challenges, typically encountered in microelectronics fabrication, have to be overcome. The Schottky diode is widely studied in the literature since it also helps evaluating the quality of semiconductor materials used for microelectronic applications.

A Schottky diode is mainly formed by a semiconductor, a Schottky contact and an ohmic contact. When a forward bias of few hundred mV is applied on the ohmic contact, the current (the carriers) starts to flow from the ohmic metal to the semiconductor and increases exponentially. Only majority carriers participate to the current conduction. The threshold voltage $V_F$ is an approximation of the Schottky barrier. Therefore, a Schottky diode shows a
lower $V_F$ compared to a bipolar one. When applying a reverse bias, the barrier height increases and the electrical field increases. Consequently, the space charge region (SCR) expands in the semiconductor. The main advantages of the Schottky diode on the bipolar one (PN) are the low $V_F$ in on-state, the low power losses and the fast switching due to the absence of minority carriers. The low power losses help reducing the heat, thus resulting in smaller radiators. Schottky diodes with a breakdown voltage ($V_{BR}$) of 600 V or 1200 V are used in PFC, applications in which the Schottky diode undergoes high frequency on off-state switching. Consequently, unipolar devices (e.g. Schottky diode) with the advantages mentioned above are favored over bipolar devices.

The major drawback of the Schottky diode is the leakage current. In fact, applying high voltages on a relatively thin active layer induces high electric field, in particular, during the off-state. The main mechanisms responsible for the leakage current are tunnel effect transport and barrier lowering (below the Schottky contact).

During the past few years, GaN Schottky diodes were developed in our laboratory. The substrates used consisted of a 2 µm GaN ($n^+$) on top of the buffer layer capped then by 5-6 µm of GaN ($n^-$). Different structures were investigated, namely, the lateral and the pseudo-vertical Schottky diodes presented in Fig. 1-15-a and b, respectively.

The lateral structure consists in a planar structure with the Schottky and the ohmic contacts at the surface while the pseudo-vertical one consists in etching under ohmic contact to reach $n^+$ type GaN. However, $n$ and $p$-type localized ion implantations are required to process such a good quality diode. The $n$-type dopants are implanted under the ohmic contact to reduce the specific contact resistivity and the $p$-type dopants are used to create guard rings around the circular Schottky contact. Consequently, these structures present many challenges to overcome.

![Fig. 1-15. (a) Lateral and (b) pseudo-vertical Schottky diodes structures on GaN-on-Si.](image-url)
The alternative solution is to process a Schottky diode on the AlGaN/GaN heterostructure. The absence of dopant is compensated by the presence of the 2DEG at the heterointerface. Consequently, the lateral current transport is maintained. Depending on the anode-cathode distance and the field plates (metal overlapping on the passivation), this structure allows to reach high breakdown voltage for Schottky diodes (up to 600 V) with no additional doping. Guard rings (p-type doping presented in Fig. 1-15) can be used in this case to increase the breakdown voltage up to 1200 V.

Fig. 1-16. Recessed lateral Schottky diode on the AlGaN/GaN heterostructure. The 2DEG appears at the heterointerface.

However, using undoped GaN leads to charge trapping and de-trapping at the insulator interfaces as well as in the bulk. In wide band gap materials, such as GaN, the traps can be located at deep levels, resulting in a trapping and de-trapping phenomena that can last up to few hours or more, depending on the voltage applied. This phenomenon, called “current collapse”, is generally considered as an undesirable “memory” effect that takes place after high voltage reverse polarization. The current degrades and the on-state resistance increases. Many solutions are proposed to suppress the current collapse such as additional p-GaN or p-AlGaN on the AlGaN layer. Indeed, current collapse can be induced by the negatively charged region which is caused by the hole emission in the epi-layer. The hole injection from the p-GaN drain compensates the trapped charges in the epi-layer. The buffer layers also contribute to the current collapse where the carriers are trapped at the interfaces of the buffer layers. Consequently, GaN:C or GaN:Mg back-barriers under the GaN channel are also considered as a solution for the current collapse. In a similar manner, the hole injection from the p-GaN drain compensates the trapped charges. Slant field plates using a slant SiCN passivation layer exhibited much less current collapse in the pulsed I-V characteristics than the device with a conventional field plate, as reported by Kobayashi et al. Field plates on the ohmic contact also reduce the current collapse. To summarize, the current collapse is considered as a road
block for GaN-based devices. The suppression of this phenomenon can pave the road to commercializing viable devices.

Up to date, no GaN Schottky diode is commercialized. Transphorm has qualified its first 600 V GaN-on-Si HEMTs in January 2013 but Schottky are not yet available. MicroGaN has commercialized normally-on switch HEMTs in which no additional elements have to be added, however, they have also proposed normally-off switch HEMTs also called “hybrid Cascode”. This device consists in a low voltage Si-MOSFET and a high voltage GaN switch HEMT. The Si-MOSFET is turning off the GaN switch while GaN switch Drain is defining the 600 V behavior of the Cascode. The last product is a low barrier diode combining a low voltage Si-SBD and a 600 V GaN-switch. This device is called SiGaN-SBD. Many technological challenges must be overcome to process a reliable Schottky diode on thick GaN. Faced to the difficulties, the alternative solution is to develop Schottky diodes on the AlGaN/GaN heterostructure.

1.4 Technological steps of GaN diodes

To process a microelectronic device such as the one previously mentioned, technological step developments are required. The simplest approach to develop high power devices on III-N materials is to transfer the technological steps developed on Si and to adapt them to these materials. However, this can be a daunting task due to the specific issues associated to III-N materials. Consequently, a detailed study of the doping, the surface treatments (native oxide and impurities removal), the recess structures as well as high breakdown voltage passivations and good ohmic and Schottky contacts, is crucial in order to process an efficient power device. Based on our previous study done in GREMAN on GaN-on-Si, few technological steps were transferred on the heterostructure and will be discussed.

1.4.1 Doping

Doping is a technological milestone in device process on these new materials. Controlling the doping level is crucial to complete a high efficient device. Doping can be achieved in-situ during the epitaxy (MOCVD, MBE or VLS) or ex-situ by ion implantation. In-situ doping is generally used for applications such as LEDs where an entire layer is doped (n or p-type doping). Ion implantation is employed when localized doping by using an adequate masking is

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3 http://www.transphormusa.com/products/
4 http://www.microgan.com/ Consulted in 2013
required. Nevertheless, impurities contaminate GaN during the epitaxy. Impurities, such as oxygen and Si, results in an unintentionally doped n-type GaN. More than that, vacancies in the GaN lattice produce “virtual” dopants. Indeed, nitrogen desorbs from GaN upon high temperature annealing. Consequently, resulting in nitrogen vacancies ($V_N$) in the GaN lattice that act also as n-type dopants. Table 1-4 gives details on the dopant elements in GaN.

<table>
<thead>
<tr>
<th>Dopant element</th>
<th>Doping type</th>
<th>Substituted element</th>
<th>Energy level (meV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>N</td>
<td>Ga</td>
<td>12-30</td>
</tr>
<tr>
<td>O</td>
<td>N</td>
<td>N</td>
<td>30</td>
</tr>
<tr>
<td>C</td>
<td>N</td>
<td>Ga</td>
<td>110-140</td>
</tr>
<tr>
<td>Ge</td>
<td>N</td>
<td>Ga</td>
<td>19</td>
</tr>
<tr>
<td>C</td>
<td>P</td>
<td>N</td>
<td>900</td>
</tr>
<tr>
<td>Si</td>
<td>P</td>
<td>N</td>
<td>224</td>
</tr>
<tr>
<td>Be</td>
<td>P</td>
<td>N</td>
<td>700</td>
</tr>
<tr>
<td>Mg</td>
<td>P</td>
<td>Ga</td>
<td>150-210</td>
</tr>
<tr>
<td>Zn</td>
<td>P</td>
<td>Ga</td>
<td>210-340</td>
</tr>
</tbody>
</table>

Table 1-4 shows that carbon, for instance, can result in n or p-type doping. Consequently, GaN containing high concentrations of carbon is self-compensated, suggesting that carbon is occupying both Ga and N sites. Furthermore, the energy level of C is lower when occupying preferentially Ga site.

The most frequently used dopants for n and p-type are Si and Mg, respectively. Intensive research on GaN doping has resulted in achieving high carrier concentration by in-situ doping. Nevertheless, local doping by ion implantation in GaN remains a critical issue. Ion implantation induces defects in GaN crystalline structure, thus, dopant activation requires firstly a recrystallization of GaN lattice, while the dopant atoms settle in substitutional sites (Ga or nitrogen sites). As a consequence, a thermal treatment at very high temperatures is necessary to reduce the defect density and to activate the implanted dopants. Nevertheless, above 820 °C, nitrogen starts to out-diffuse from GaN and the surface is damaged. When increasing the annealing temperature, surface roughness increases, dislocations and hexagonal pits are brought to light and finally for the highest temperatures, GaN material is destroyed. Then, it is obviously impossible to process a reliable device on such a surface, especially Schottky contacts which are highly sensitive to surface state. Faced to these difficulties, the protection of GaN during thermal treatment with a cap-layer is essential. Cap-layers and high temperature thermal treatments will be discussed in Chapter 4.
1.4.2 Surface treatments

Impurities and native oxide removal prior to any metal or passivation layer deposition is crucial to fabricate reliable devices. Consequently, the surface treatment is essential prior to any deposition on the semiconductor surface. To do so, wet chemical or dry (plasma) surface treatments are of high relevance. Both treatments can be combined in some cases.

➢ GaN chemical treatment

Organic or metallic impurities and gallium oxide (native oxide) removal prior to any metal or passivation deposition is crucial to fabricate reproducible and reliable devices on GaN. Hydrofluoric, hydrochloric acid and ammonium hydroxide are known to eliminate GaN native oxide $^{13,35}$. Hashizume et al. $^{35}$ have showed by X-ray photoelectron spectroscopy that air-exposed GaN surface is covered with a natural oxide layer including large amounts of Ga-oxide. They have reported a significant decrease in the oxide components (O1s peak) after NH$_4$OH treatment. Standard clean 1 (H$_2$O:NH$_4$OH:H$_2$O$_2$) is used to remove organic and some metallic contaminants from the surface. Table 1-5 summarizes some chemical cleanings employed by different groups of researchers.

<table>
<thead>
<tr>
<th>Solutions</th>
<th>Concentration</th>
<th>Temperature (°C)</th>
<th>Time</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCl + BOE</td>
<td>-</td>
<td>-</td>
<td>30s + 5s</td>
<td>13</td>
</tr>
<tr>
<td>HCl:HF:H$_2$O</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>36,37</td>
</tr>
<tr>
<td>(NH$_4$)$_2$S</td>
<td>-</td>
<td>boiling</td>
<td>20 m</td>
<td>38</td>
</tr>
<tr>
<td>Acetone+methanol+IPA + H$_2$SO$_4$:H$_2$O$_2$</td>
<td>1:1</td>
<td>110</td>
<td>5 s</td>
<td>39</td>
</tr>
<tr>
<td>H$_2$O:NH$_4$OH:H$_2$O$_2$</td>
<td>6:1:1</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>H$_2$O:HCl:H$_2$O$_2$</td>
<td>6:1:1</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>BHF</td>
<td>-</td>
<td>-</td>
<td>2 m</td>
<td>41,42</td>
</tr>
<tr>
<td>HNO$_3$:HCl + KOH + Boiling</td>
<td>1:3</td>
<td>-</td>
<td>-</td>
<td>43</td>
</tr>
<tr>
<td>BOE</td>
<td>6:1</td>
<td>-</td>
<td>15 s</td>
<td>44</td>
</tr>
<tr>
<td>NH$_4$OH</td>
<td>-</td>
<td>50°C</td>
<td>60 s</td>
<td>45</td>
</tr>
<tr>
<td>Organic solvents</td>
<td>-</td>
<td>-</td>
<td>15 m</td>
<td>35</td>
</tr>
<tr>
<td>NH$_4$OH</td>
<td>-</td>
<td>20-50°C</td>
<td>5-15 m</td>
<td></td>
</tr>
</tbody>
</table>

➢ GaN plasma treatment

Plasma pretreatments have been reported using O$_2$ $^{46,47}$, NH$_3$ $^{46,48}$, N$_2$ $^{45,46}$, Cl$_2$-based inductively coupled plasma (ICP) $^{49,50}$. This treatment improves the device performance (e.g. before passivation deposition). Romero et al. $^{45}$ have reported on the use of N$_2$ pretreatment in HEMT
passivation. They have reported the reduction of current collapse and gate-lag effects. Edwards et al. 48 have reported the same effects on current collapse and gate-lag when using NH$_3$ pretreatment prior to SiN$_x$ deposition. Li et al. 50 have reported on N$_2$ and BCl$_3$/Cl$_2$ plasma treatment on n-GaN. They have reported an improvement in the specific contact resistance after BCl$_3$/Cl$_2$ treatment compared to N$_2$ treatment.

Consequently, surface treatment improves the electrical performance of the device through native oxide or impurity removal from the surface or through nitridation the surface prior to the passivation deposition.

### 1.4.3 Heterostructure recess

As explained earlier, the 2DEG is formed at 5 to 10 nm in the GaN layer at the interface with AlGaN. With the presence of 20-30 nm of AlGaN and 2-3 nm of GaN cap-layer and, in some cases, 100-200 nm of SiN$_x$ above the 2DEG, the recess of these layers is necessary for both contacts. Different types of recess exist in the literature generally called: shallow, partial and full recesses$^{39,51,52}$. While the shallow and the partial recesses consist of etching the SiN$_x$ layer (if any), the GaN cap-layer and few nm of AlGaN, leaving behind a sufficient AlGaN thickness (> t$_{CR}$) to create the 2DEG at the interface (c.f. Fig. 1-9), the full recess results in the removal of all AlGaN layer and few nm of GaN under the contacts. Thus, the metal deposited is in a lateral contact with the 2DEG. Wang et al. 53 have reported on low ohmic contact resistance (Rc of 0.26 Ω.mm) using a recessed structure. They have also reported that low Rc were obtained only when the 2DEG channels were completely removed under the ohmic contacts. Fig. 1-17 shows a cross sectional schematic of the shallow, the partial and the full recesses.

![Fig. 1-17. Cross sectional view of (a) shallow, (b) partial and (c) full recess, from left to right. The 2DEG appears at the AlGaN/GaN interface.](image)

GaN layers can be chemically etched in boiling KOH $^{54}$ or H$_3$PO$_4$ $^{55,56}$. However, chemical etching is an unsuitable solution to perform the recess since it is difficult to control the etch rate.
(at the nm scale). The only alternative is the dry etching (plasma). Reactive ion etching (RIE) is the most used technique to perform the recess. RIE technique combines physical etching due to the accelerated ion bombardment and chemical etching due to species introduces in the chamber. SF₆, BCl₃, Cl₂ are the most used species to etch GaN. GaN contamination by F and Cl when using RIE is still debated. Even though most of the literature mention GaN etch using RIE, ion beam etching (IBE) is an interesting alternative. IBE consists of creating plasma using Ar ions without any chemical species. Furthermore, etching at very low rate (2 nm.min⁻¹) is possible making the recess depth precisely controllable.

1.4.4 Dielectric passivations

Dielectric passivations have more than one purpose. They protect GaN surface during all the process steps (ion implantation, etching, thermal treatments...). They are also expected to isolate electrically the contacts (e.g. 600 V Schottky diode with L_AC of 15 µm) and reduces the interface charges. Consequently, the passivation breakdown field has to be higher than the one of GaN (3.3 MV/cm). Many passivations have been already mentioned in the literature such as SiO₂, Si₃N₄, AlN, Al₂O₃, MgO and more deposited by different techniques (plasma enhanced chemical vapor deposition - PECVD, low pressure chemical vapor deposition - LPCVD, MOCVD etc.). Yagi et al. have reported on ebeam deposition of SiNx, SiO₂ and TiO₂ passivation films used as insulator in metal-insulator-semiconductor gate on AlGaN/GaN HEMT structure with a sheet resistance between 420-510 Ω/□. They have found the sheet resistance to be 512, 628 and 992 Ω/□ for the SiNx, SiO₂ and TiO₂ films, respectively, and have considered that the surface passivation using the TiO₂ and SiO₂ films reduces the carrier density in the AlGaN/GaN channel.

However, one of the most used passivation on the heterostructure is silicon nitride deposited by different techniques from in-situ epitaxy to LPCVD and PECVD. The SiNx passivation layer shows a low interface trap density and high breakdown voltage greater than 2 MV.cm⁻¹.

Hua et al. have studied PECVD and LPCVD-SiNx gate dielectrics for GaN-based metal-insulator-semiconductor HEMTs. They have reported a lower reverse gate leakage, a higher forward gate breakdown voltage and a lower ON-resistance for the LPCVD-SiNx. However, no difference in current collapse suppression between PECVD and LPCVD-SiNx has been observed.
Consequently, a high-quality passivation layer is required to achieve low ON-resistance and high breakdown voltage device.

### 1.4.5 Contacts

#### 1.4.5.1 Ohmic contact

Based on the band theory, a good ohmic contact on any semiconductor must have a relatively low work function, compared to the one of the semiconductor, thus resulting in a low barrier height at the interface metal/semiconductor. The electron transport will face this barrier and consequently occurs with a very low resistance. Since the 90s, the ohmic contacts on GaN have been developed. The simplest approach was to transfer the ohmic metal on GaN to AlGaN/GaN heterostructure. In general, the metal stack consists of 3 to 4 metal layers. The first bilayer is usually Ti/Al. Au-containing metal stack are formed by Ti/Al/X/Au, where X is Ni, Ti, Ta, Mo, Pt, V... Au is suggested to prevent the metal surface oxidation, while X is used to prevent Au diffusion into the semiconductor. Table 1-6 summarizes the literature results reported on ohmic contacts on AlGaN/GaN heterostructure. AlGaN composition/thickness, the metal stack and annealing and the electrical results are presented.
Table 1-6. Ohmic contacts on AlGaN/GaN heterostructure and the resulting contact resistance according to the literature.

<table>
<thead>
<tr>
<th>Metal layers (nm)</th>
<th>$x_{\text{Al}}$ (%)</th>
<th>$t_{\text{AlGaN}}$ (nm)</th>
<th>Annealing conditions</th>
<th>$R_c$ ($\Omega \cdot \text{mm}$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti/Al (70/200 nm)</td>
<td>-</td>
<td>25</td>
<td>500 °C for 60 sec in Ar</td>
<td>1.8</td>
<td>67</td>
</tr>
<tr>
<td>Ti/Al (70/200 nm)</td>
<td>26%</td>
<td>15</td>
<td>500 °C for 60 sec in Ar, 800 °C for 60 sec in Ar</td>
<td>10±1.8, 11.3±0.3</td>
<td>68</td>
</tr>
<tr>
<td>Ti/Al (40/200 nm)</td>
<td>-</td>
<td>25</td>
<td>550 °C for 60 sec in N$_2$</td>
<td>0.76</td>
<td>39</td>
</tr>
<tr>
<td>Ti/Al (25/105 nm)</td>
<td>26%</td>
<td>18</td>
<td>850 °C for 60 sec in Ar</td>
<td>-</td>
<td>43</td>
</tr>
<tr>
<td>Ti/Al/W (60/100/30 nm)</td>
<td>26%</td>
<td>17.5</td>
<td>870 °C for 30 sec</td>
<td>0.49</td>
<td>51</td>
</tr>
<tr>
<td>Ti/Al/TiN (0.05/4/60 nm)</td>
<td>20%</td>
<td>15</td>
<td>550 °C for 90 sec in N$_2$</td>
<td>0.62</td>
<td>69</td>
</tr>
<tr>
<td>Ti/Al/Ti/TiN (20/200/20/60 nm)</td>
<td>21%</td>
<td>15</td>
<td>550 °C</td>
<td>1.5</td>
<td>70</td>
</tr>
<tr>
<td>Ta/Al/Ta (10/280/20 nm)</td>
<td>14%</td>
<td>22</td>
<td>550 °C for 60 sec</td>
<td>0.06</td>
<td>40</td>
</tr>
<tr>
<td>Ta/Al/Ni/Au (10/140/40/40 nm)</td>
<td>14%</td>
<td>22</td>
<td>550 °C for 60 sec</td>
<td>0.28</td>
<td>40</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au (20/105/50/150 nm)</td>
<td>26%</td>
<td>30</td>
<td>890 °C for 30 sec in N$_2$</td>
<td>2.85</td>
<td>20</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au (15/100/50/50 nm)</td>
<td>32%</td>
<td>23</td>
<td>875 °C for 60 sec</td>
<td>0.4</td>
<td>46</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au (10/200/45/55 nm)</td>
<td>25%</td>
<td>25</td>
<td>800 °C in N$_2$</td>
<td>0.8</td>
<td>71</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au (20/72/12/40 nm)</td>
<td>26%</td>
<td>25</td>
<td>750 °C for 30 sec</td>
<td>1.23</td>
<td>72</td>
</tr>
<tr>
<td>Si/Ti/Al/Mo/Au (5/20/60/35/50 nm)</td>
<td>25%</td>
<td>20</td>
<td>830 °C for 30 sec in N$_2$</td>
<td>0.6</td>
<td>73</td>
</tr>
<tr>
<td>Ti/Al/Mo/Au (15/60/35/50 nm)</td>
<td>30%</td>
<td>21.5</td>
<td>850 °C for 30 sec</td>
<td>-</td>
<td>74</td>
</tr>
<tr>
<td>Ti/Al/Mo/Au (15/60/35/50 nm)</td>
<td>30%</td>
<td>20</td>
<td>850 °C for 30 sec in N$_2$</td>
<td>0.26</td>
<td>53</td>
</tr>
<tr>
<td>Ti/Al/Mo/Au (15/60/35/50 nm)</td>
<td>20%</td>
<td>25</td>
<td>800 °C in N$_2$</td>
<td>0.38</td>
<td>75</td>
</tr>
<tr>
<td>Mo/Al/Mo/Au (15/60/35/50 nm)</td>
<td>20%</td>
<td>25</td>
<td>650-800 °C in N$_2$</td>
<td>0.22</td>
<td>75</td>
</tr>
<tr>
<td>V/Al/Mo/Au (15/60/35/50 nm)</td>
<td>20%</td>
<td>25</td>
<td>700 °C in N$_2$</td>
<td>0.35</td>
<td>75</td>
</tr>
<tr>
<td>V/Al/Pt/Au (15/85/50/50 nm)</td>
<td>30%</td>
<td>7.5</td>
<td>650 °C for 45 sec in N$_2$</td>
<td>0.82</td>
<td>76</td>
</tr>
<tr>
<td>Ti/Al/Pt/Au (15/85/50/50 nm)</td>
<td>30%</td>
<td>7.5</td>
<td>850 °C for 60 sec in N$_2$</td>
<td>0.51</td>
<td>76</td>
</tr>
</tbody>
</table>
Ohmic contact choice depends on the device application. For the rectifiers to be compatible with CMOS technology, Au-free contacts are mandatory since Au contaminates Si by forming energy traps. They also represent a low-cost process, consequently, answering to a criterion of market’s demand.

1.4.5.2 Schottky contact

Unlike ohmic contact, Schottky contact work function should be higher than the one of the n-type semiconductor. A high barrier height will be then formed at the interface metal/semiconductor. This barrier must have the capability to block the electron flow in one way, even for the high voltages applied (> 600 V), and should have the lowest resistance to carriers, for a given polarization. It is well known that the metal work function has an impact on Schottky barrier height ($q\Phi_B$). In general, metals with work function higher than 4.5 eV are potential candidates to form Schottky barriers on the AlGaN/GaN heterostructure. Table 1-7 summarizes metal work function and electronegativity from ref 3,44,77–83.

<table>
<thead>
<tr>
<th>Metal</th>
<th>Metal work function (eV)</th>
<th>Metal electronegativity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt</td>
<td>5.65</td>
<td>2.2</td>
</tr>
<tr>
<td>Pd</td>
<td>5.12</td>
<td>2.2</td>
</tr>
<tr>
<td>Au</td>
<td>5.1</td>
<td>2.4</td>
</tr>
<tr>
<td>Ti</td>
<td>4.33</td>
<td>1.5</td>
</tr>
<tr>
<td>Ni</td>
<td>5.15</td>
<td>1.8</td>
</tr>
<tr>
<td>Cr</td>
<td>4.5</td>
<td>1.6</td>
</tr>
<tr>
<td>Pb</td>
<td>4.25</td>
<td>1.8</td>
</tr>
<tr>
<td>Ag</td>
<td>4.26</td>
<td>1.9</td>
</tr>
<tr>
<td>Ir</td>
<td>5.46</td>
<td>2.2</td>
</tr>
<tr>
<td>Rh</td>
<td>5.0</td>
<td>2.2</td>
</tr>
<tr>
<td>Ru</td>
<td>4.7</td>
<td>2.2</td>
</tr>
<tr>
<td>Co</td>
<td>5.0</td>
<td>1.8</td>
</tr>
<tr>
<td>Mo</td>
<td>4.6</td>
<td>2.1</td>
</tr>
<tr>
<td>Cu</td>
<td>4.65</td>
<td>1.9</td>
</tr>
<tr>
<td>W</td>
<td>4.5 eV</td>
<td>2.3</td>
</tr>
<tr>
<td>W$_2$N</td>
<td>4.62 eV</td>
<td>-</td>
</tr>
</tbody>
</table>

Using AlGaN/GaN heterostructure, Schottky barrier height is also influenced by other parameters such as the heteroepitaxy quality, the surface treatments or roughness. Furthermore, AlGaN thickness not only influences the 2DEG density but also the barrier height $q\Phi_B$.  

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Consequently, anode recess (discussed in 1.3.3) affects $q\Phi_B$. Treidel et al. 84 have reported on $q\Phi_B$ using recessed and planar anodes on AlGaN/GaN. They have reported the decrease in $q\Phi_B$ when recessing AlGaN and explained this drop by the 2DEG contact with the anode metal.

Single and multi-metal layers can be used to form a Schottky barrier on the heterostructure as shown in Table 1-8. Barriers vary from 0.6 to 1.68 eV for an ideality factor between 1 and 5.
Table 1-8. Schottky contacts on AlGaN/GaN heterostructure with the corresponding annealing/recess and the resulting Schottky barrier $\Phi_B$ and ideality factor according to the literature.

<table>
<thead>
<tr>
<th>Metal layers</th>
<th>$x_{\text{Al}}$ (%)</th>
<th>$t_{\text{AlGaN}}$ (nm)</th>
<th>Annealing recess conditions</th>
<th>$q\Phi_B$ (eV)</th>
<th>Ideality factor</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt/Ti/Au</td>
<td>25%</td>
<td>25 nm</td>
<td>No recess</td>
<td>0.62 eV</td>
<td>1.67</td>
<td>84</td>
</tr>
<tr>
<td>Ni/Pt/Au (20/20/360 nm)</td>
<td>23%</td>
<td>20 nm</td>
<td></td>
<td></td>
<td></td>
<td>85</td>
</tr>
<tr>
<td>Ni/Au (40/120 nm)</td>
<td>-</td>
<td>-</td>
<td></td>
<td>1.35 eV</td>
<td>-</td>
<td>57</td>
</tr>
<tr>
<td>Ni/Au</td>
<td>-</td>
<td>30 nm</td>
<td></td>
<td>0.9 eV</td>
<td>-</td>
<td>86</td>
</tr>
<tr>
<td>Ni/Au (40/130 nm)</td>
<td>20%</td>
<td>20 nm</td>
<td>430 °C in N$_2$</td>
<td>0.68-0.71 eV</td>
<td>-</td>
<td>87</td>
</tr>
<tr>
<td>Ni/Au (50/150 nm)</td>
<td>26%</td>
<td>30 nm</td>
<td>&gt; 400 °C$^5$</td>
<td>-</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Ni/Au (20/300 nm)</td>
<td>25%</td>
<td>20 nm</td>
<td>Partial recess (5 nm AlGaN left)</td>
<td>-</td>
<td>-</td>
<td>13</td>
</tr>
<tr>
<td>Ni/Au (50/500 nm)</td>
<td>23%</td>
<td>20 nm</td>
<td></td>
<td>-</td>
<td>-</td>
<td>88</td>
</tr>
<tr>
<td>Ni/Au (60/160 nm)</td>
<td>28%</td>
<td>22.5 nm</td>
<td>(Rectangular diode)</td>
<td>1.20 eV</td>
<td>5.77</td>
<td>89,90</td>
</tr>
<tr>
<td>Ni/Au (50500 nm)</td>
<td>23%</td>
<td>20 nm</td>
<td>(Circular diode)</td>
<td>1.39 eV</td>
<td>3.62</td>
<td></td>
</tr>
<tr>
<td>Ni/Au (30/50 nm)</td>
<td>26%</td>
<td>18 nm</td>
<td></td>
<td>1.02 eV</td>
<td>1.34</td>
<td>43</td>
</tr>
<tr>
<td>Ni/Au (60/300 nm)</td>
<td>25%</td>
<td>20 nm</td>
<td></td>
<td>1.27 eV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ir (150 nm)</td>
<td>25%</td>
<td>20 nm</td>
<td></td>
<td>1.12 eV</td>
<td>-</td>
<td>91</td>
</tr>
<tr>
<td>Re (200 nm)</td>
<td>-</td>
<td>-</td>
<td></td>
<td>1.68 eV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ir (35 nm)</td>
<td>10%</td>
<td>1 µm</td>
<td>850 °C for 30 sec</td>
<td>1.21 eV</td>
<td>1.24</td>
<td>92</td>
</tr>
<tr>
<td></td>
<td>20%</td>
<td></td>
<td></td>
<td>1.4 eV</td>
<td>1.16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25%</td>
<td></td>
<td></td>
<td>1.45 eV</td>
<td>1.18</td>
<td></td>
</tr>
<tr>
<td>Ti (100nm)</td>
<td>11%</td>
<td>300 nm</td>
<td>300 °C in N$_2$</td>
<td>0.6 eV</td>
<td>1.10</td>
<td>93</td>
</tr>
<tr>
<td>Pd (100 nm)</td>
<td>11%</td>
<td>300 nm</td>
<td>300 °C in N$_2$</td>
<td>0.95 eV</td>
<td>1.27</td>
<td></td>
</tr>
<tr>
<td>Ni (100 nm)</td>
<td>-</td>
<td>-</td>
<td></td>
<td>0.97 eV</td>
<td>1.38</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>-</td>
<td>-</td>
<td></td>
<td>0.89 eV</td>
<td>1.15</td>
<td></td>
</tr>
<tr>
<td>WN$_x$ Ni/Au (20/200 nm)</td>
<td>25%</td>
<td>30 nm</td>
<td>-</td>
<td>1.21 eV</td>
<td>1.24</td>
<td>83</td>
</tr>
<tr>
<td>TiN/Ti/Al/Ti/TiN (20/20/250/20/60 nm)</td>
<td>21%</td>
<td>15 nm</td>
<td>550 °C Partial recess (5 nm AlGaN left)</td>
<td>0.56 eV</td>
<td>1.33</td>
<td>58,70</td>
</tr>
</tbody>
</table>

$^5$ Samples annealed at 400 °C for 10 min to repair implantation induced damages (after Ni Au evaporation).
1.5 Objectives of this research work

This work focuses on the development of a Schottky diode on the heterostructure AlGaN/GaN on Si. The work is supported by Bpi France under the “Programme Investissement d’Avenir” (PIA) “Tours 2015” where STMicroelectronics and laboratories work together on the epitaxy, diodes process and simulation, GaN etching etc.

Our work focuses on the development of technological steps such as ohmic and Schottky contacts, silicon nitride passivations, III-N etching (for recessed structures), cap-layers and dopant activation. These components will be discussed in details in the following chapters.

Different material epitaxies (from different suppliers) are used to process Schottky diodes. The AlGaN/GaN heterostructure was provided by supplier C (main supplier and partner in the project “Tours 2015”) on 8 in. Si (111) substrates, while the other heterostructures were epitaxied on 6 in. Si (111) substrates, by different suppliers (called A and B for confidential reasons).

The work presented in the scope of this manuscript led to the fabrication of high breakdown voltages (> 600 V) Schottky diodes based on these heterostructures. The Schottky recess, surface treatment and annealing temperatures are studied. The distance anode-cathode and the field plates length are also treated as parameters. Later on, the electrical characteristics of these diodes are discussed in details.

1.6 Conclusions

In this chapter, we presented the crystalline structure of III-N, especially Wurtzite GaN. We discussed the MOCVD epitaxy of GaN and the substrate choice. We concluded that GaN-on-Si was the solution for a low cost technology. MOCVD is the most used deposition technique for industrial purpose based on the good epitaxy quality and high rate deposition. We depicted the ternary alloy AlGaN and the corresponding polarization when epitaxied on GaN, the formation of the 2DEG and its mobility and density. Compared to GaN, the AlGaN/GaN heterostructure presents the benefit of a high mobility and high density 2DEG at the interface without any dopant incorporation.

The second section brought up the topic of GaN-based devices such as HEMTs and Schottky diodes. The channel of conventional HEMTs is populated with electrons, thus, the HEMTs are
working in normally-on mode. However, normally-off mode HEMTs are required for high power switches. Modified structures to obtain a normally-off HEMTs have been proposed. We also discussed the main advantages of Schottky diodes, used in power converters, compared to bipolar ones. Two different diodes structures on thick GaN epitaxied on Si were presented and compared to their alternative solution, Schottky diodes on AlGaN/GaN/Si. This part also focused on commercialized devices for high power applications.

The third section of this chapter described the technological steps to realize a Schottky diode on the heterostructure. The doping, the surface treatments, the recess, the passivation layer, and especially the contacts (ohmic and Schottky) were discussed, based on the literature results. We concluded that the protection of implanted GaN surface during high temperature thermal treatments (for dopant activation) is essential, the surface treatments and the recess are necessary before any contact or passivation deposition, the dielectric layer, such as SiN$_x$ layer, is essential for high voltage breakdown and finally, the importance of Au-free ohmic and Schottky contacts compatible with CMOS technology and also low cost solution.

Finally, the last section focused on the purpose of this thesis which deals with the process of high breakdown voltage Schottky diode on the AlGaN/GaN heterostructure targeting PFC.

The following chapter explains the technological steps and will focus on the ohmic and Schottky contacts, passivations, recessed structures. Fabricated ohmic and Schottky with or without passivations on recessed and recess-free structures are electrically characterized.
Chapter 2. Technological steps development:

contacts, passivation and recess study
GaN has been studied since the 90s to process LEDs or laser diodes. However, GaN has recently attracted researchers attention to high power devices, as already mentioned. In particular, Schottky diodes were developed in GREMAN in collaboration with STMicroelectronics, OMMC, SOITEC and CRHEA laboratory (G²Rec project). Due to the difficulties faced during the process of GaN-based Schottky diodes, interest for AlGaN/GaN heterostructure for high power applications also appeared. The presence of a thin AlGaN barrier and the 2DEG at the AlGaN/GaN interface make the Schottky diode process slightly different than the pseudo vertical one on thick GaN. A simple approach would have been to transfer the technological steps previously developed on GaN to AlGaN/GaN heterostructure, but in reality, the technology transfer is not that simple.

This chapter is dedicated to technological steps development for Schottky diode on the AlGaN/GaN heterostructure. As discussed in section 1.4, to reach high breakdown voltage and low leakage current Schottky diodes, an adequate passivation layer and excellent ohmic and Schottky contacts are required.

First, we show the different material heterostructures provided by different suppliers. The surface and the crystalline characterizations are presented.

The second part focuses on the SiNx passivation layer obtained by PECVD. The deposition conditions are presented and the layer characterizations are discussed.

The third and fourth parts represent the main contribution to this chapter and concern the ohmic and Schottky contacts, respectively. The electrical characterizations of the ohmic contacts by means of transfer length method (TLM) are presented. The different parameters affecting the electrical results are studied, mainly Al metal layer thickness, surface treatments, annealing temperatures and, also recess process. This study allows to conclude on a good and repeatable ohmic contact. A comparison between the different epitaxies is also presented as a function of the surface treatments and annealings. The Schottky contacts study evidence the lowest leakage current density when using a triple combination of annealing-recess-passivation optimization. These results will be used for the diode process presented in Chapter 3.
2.1 Characterization of heterostructures provided by different suppliers

The heterostructures were provided by three different suppliers using MOCVD epitaxy on Si. As part of the project “Tours 2015”, supplier C epitaxied AlGaN/GaN on 8 in. Si (111) wafers. Furthermore, two different epitaxies (C-I and C-II) were employed in our study. Two other suppliers “A” and “B” (names kept confidential) provided the epitaxy on 6 in. Si (111) wafers. All heterostructures were characterized by atomic force microscopy (AFM) and X-ray diffraction (XRD) in direct and reciprocal space.

2.1.1 Surface morphology characterization

First, we have characterized the surface morphology of the available epitaxies. Fig. 2-1 represents 10x10 µm² and 2x2 µm² AFM images in plane-view of all suppliers. C-I epitaxy (without final GaN cap-layer) shows that the AlGaN surface is teared. This teared surface is attributed to the temperature cooling down after the high temperature epitaxy. On the other hand, C-II epitaxy shows a smoother surface due to the presence of this final GaN cap-layer. The atomic steps are visible and the surface roughness of 0.55 nm, for 10x10 µm² images, can be considered as low (Table 2-1). However, high dislocation densities are revealed at the surface. Supplier A epitaxy shows the same characteristics as C-II epitaxy. The atomic steps are visible on the smooth surface with 0.67 nm roughness (Table 2-1). High dislocation density is also revealed at the surface. Finally, supplier B epitaxy also results in a smooth surface (0.65 nm roughness presented in Table 2-1) with visible atomic steps. Dislocations are hardly visible at the surface.
2.1.2 Structural characterization: XRD in plane scans

XRD in plane scans is used to characterize the crystalline quality of the different epitaxies as shown in Fig. 2-2. One can see Si (111) and GaN (000l) peaks in addition to the different buffer layer peaks. The full width at half maximum (FWHM) of GaN (0002) are reported in Table 2-1. In fact, the defects in the material, such as dislocations, are reflected in a broaden peak. Consequently, a low FWHM indicates a better crystalline quality. The largest FWHM is obtained for supplier A epitaxy, followed by supplier C (C-I and C-II) epitaxy with a FWHM of approximately 0.17 °. The lowest GaN FWHM was obtained for supplier B with a value at about 0.159 °. With the exception of supplier A, the FWHM of the other epitaxies are slightly better than the one generally found in the literature \(^ {68,94,95} \) (between 0.18 and 0.25 °).

Table 2-1. Characteristics of the different epitaxies used in this study.

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Substrate information</th>
<th>AlGaN barrier thickness (nm)</th>
<th>Al composition (%)</th>
<th>GaN cap-layer</th>
<th>Surface roughness (nm)</th>
<th>FWHM of GaN (0002) (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Si 6 in.</td>
<td>19.5</td>
<td>25</td>
<td>Confidential</td>
<td>0.67</td>
<td>0.16</td>
</tr>
<tr>
<td>B</td>
<td>Si 6 in.</td>
<td>18</td>
<td>26</td>
<td>Confidential</td>
<td>0.65</td>
<td>0.17</td>
</tr>
<tr>
<td>C-I</td>
<td>Si 8 in.</td>
<td>24</td>
<td>21.5</td>
<td>No cap</td>
<td>0.65</td>
<td>0.32</td>
</tr>
<tr>
<td>C-II</td>
<td>Si 8 in.</td>
<td>26-29</td>
<td>24</td>
<td>Confidential</td>
<td>0.55</td>
<td>0.17</td>
</tr>
</tbody>
</table>
2.1.3 Structural characterization: Reciprocal space mapping

XRD in plane scans does not supply enough information on strain and lattice relaxation of the epilayer since the epitaxy follows the c-axis and the diffracting peaks in the (000l) direction. To overcome these difficulties, XRD in the reciprocal space, also called reciprocal space mapping (RSM), helps characterizing the epitaxies according to any direction. This technique consists in a 2θ-ω scans. The sample is rotated by ω and the detector is rotated by 2θ. For each ω variation, the detector scans a 2θ±5°. The scans are slow and can take up to 10 hours. Finally, 2θ is plotted against ω and the graph is converted to “qz” and “qx”, as can be seen in Fig. 2-3. “qz” and “qx” (in nm⁻¹) are related to the lattice parameters “c” and “a”, respectively. Thus, from the center of each spot in Fig. 2-3, one can extract the lattice parameters of the layer.

In our study, we compare the different RSMs of all suppliers in order to estimate the strain of each epitaxy. Since GaN is hexagonal, the four Miller-Bravais indices (hkil) are used to describe the planes in the crystal, where i = - (h + k). One of the accessible reflections of GaN is the (-1-124) which is used in this study. This reflection helps finding the lattice parameters of GaN and of the buffer layers. It is important to remind that the role of the buffer layers is to reduce
the lattice mismatch between the substrate (Si, in our case) and the GaN epilayer. Consequently, three different possibilities can take place: Unstrained, fully strained or residually strained (partially relaxed) buffer layers. Both lattice parameter “a” and “c” may vary according to the strain. In the case of a fully strained structure, the buffer layers RSM is aligned with GaN one according to “q_x” axis. The in-plane lattice parameter is close to the GaN one. For instance, an AlN layer in this structure has a lattice parameter “a” closer to the GaN one rather than to the AlN one. In the other cases (partially or totally relaxed structures), the lattice parameter “a” of the buffer layers is equal or closer to that of the corresponding material (AlN or AlGaN). Fig. 2-3 represents the RSM of (-1-124) diffraction of the epitaxied wurtzite layers. The RSM of all suppliers mentioned in Table 2-1 are also featured in Fig. 2-3. The intensity increases from white to blue, red, yellow and black meaning that the black spot corresponds to the thickest layer, GaN.

Fig. 2-3. RSM of GaN (-1-124) diffraction and the corresponding buffer layers. The white rectangles hiding the buffer layers of the corresponding structures are used for confidential issues related to suppliers A and B.
A slight difference between the different epitaxies of supplier C (partner in our study) is observed. The buffer layer epitaxy has slightly changed. However, GaN layer strain remains unchanged. On the other hand, the structure is in a partial relaxation since the lattice parameter “a” of the buffer layers is different than the one of GaN. Table 2-2 compares GaN and AlN lattice parameters extracted from RSM to theoretical ones. GaN seems to be fully relaxed with lattice parameters close or equal to theoretical ones. However, “a” of epitaxied AlN is higher than theoretical one and “c” is lower resulting in a strained layer.

Table 2-2. Lattice parameters of GaN and AlN extracted from RSM.

<table>
<thead>
<tr>
<th>Supplier</th>
<th>GaN</th>
<th>AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>a (Å)</td>
<td>c (Å)</td>
</tr>
<tr>
<td>Theoretical</td>
<td>3.189</td>
<td>5.185</td>
</tr>
<tr>
<td>Supplier A</td>
<td>3.189</td>
<td>5.186</td>
</tr>
<tr>
<td>Supplier B</td>
<td>3.188</td>
<td>5.186</td>
</tr>
<tr>
<td>Supplier C-I</td>
<td>3.189</td>
<td>5.185</td>
</tr>
<tr>
<td>Supplier C-II</td>
<td>3.186</td>
<td>5.186</td>
</tr>
</tbody>
</table>

We can notice from Table 2-2 that the wafers provided by Supplier A are similar to those provided by Supplier C. GaN lattice parameters are close to theoretical ones resulting in a relaxed layer as shown in Fig. 2-3. The AlN layer epitaxied by supplier A is in strain. On the other hand, supplier B uses a super lattice buffer layer resulting in a strained structure, while the GaN layer is relaxed. Consequently, depending on the buffer layer and the epitaxy conditions, the strain of the epitaxied layers varies. Greco et al. 96 have reported on a correlation between the material quality and the ohmic contact on the AlGaN/ GaN heterostructures grown on Si substrate. The strained epitaxy (supplier B) results in a higher density 2DEG. Consequently, we expect electrical results variation depending on the epitaxy quality.

### 2.2 Passivation study for the heterostructure

To achieve low leakage current and high breakdown voltage diodes, good surface passivation is crucial prior to any process step. Consequently, the reduction of interface charges can be the key parameter to reach highly efficient devices. SiOₓ is the most commonly used passivation layer in the semiconductor field. However, in the case of AlGaN/GaN heterostructure, SiOₓ presents many drawbacks such as the presence of oxygen that can act as a donor in III-N materials. An alternative passivation material is silicon nitride used also in planar devices. The main advantages of SiNₓ over SiOₓ is this absence of O and its higher dielectric constant. SiNₓ
is also chemically stable resulting in a material of choice for passivation. In this manuscript, we study the PECVD deposition conditions for an efficient SiN\textsubscript{x} layer.

### 2.2.1 PECVD silicon nitride deposition

SiN\textsubscript{x} deposited by PECVD has been chosen as a passivation layer. Several parameters can be tuned during PECVD process, such as low and high frequency power (LF and RF, respectively), temperature, pressure, deposition time, SiH\textsubscript{4} and NH\textsubscript{3} ratio and gas flow. GREMAN and STMicroelectronics have contributed to the development of SiN\textsubscript{x} layers grown by PECVD in CERTeM clean room. Consequently, based on these previous results and the literature ones \(^97-106\), we proposed the following experiments. The layer deposition rate, refractive index and stress are mainly affected by the plasma power, the gas ratio and the total flow. The temperature also affects the layer quality. However, we fixed the temperature to 400 °C, highest temperature of our equipment, giving generally the best layer quality. Many other parameters were also fixed, such as, LF power, pressure and deposition time and are shown in Table 2-3.

<table>
<thead>
<tr>
<th>LF power (W)</th>
<th>Temperature (°C)</th>
<th>Pressure (mTorr)</th>
<th>N\textsubscript{2} gas flow (sccm)</th>
<th>Deposition time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>160</td>
<td>400</td>
<td>1800</td>
<td>1071</td>
<td>5</td>
</tr>
</tbody>
</table>

The tuned parameters are listed in Table 2-4.

<table>
<thead>
<tr>
<th>Deposition number</th>
<th>RF power (W)</th>
<th>SiH\textsubscript{4}:NH\textsubscript{3} ratio</th>
<th>SiH\textsubscript{4} gas flow (sccm)</th>
<th>NH\textsubscript{3} gas flow (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN-1</td>
<td>200</td>
<td>1:3</td>
<td>15</td>
<td>45</td>
</tr>
<tr>
<td>SiN-2</td>
<td>350</td>
<td>1:3</td>
<td>15</td>
<td>45</td>
</tr>
<tr>
<td>SiN-3</td>
<td></td>
<td>1:1</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>SiN-4</td>
<td></td>
<td>1:1</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>SiN-5</td>
<td></td>
<td>1:3</td>
<td>10</td>
<td>30</td>
</tr>
<tr>
<td>SiN-6</td>
<td></td>
<td>1:3</td>
<td>15</td>
<td>45</td>
</tr>
<tr>
<td>SiN-7</td>
<td>500</td>
<td>1:2</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>SiN-8</td>
<td></td>
<td>1:2</td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td>SiN-9</td>
<td></td>
<td>1:1</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>SiN-10</td>
<td></td>
<td>1:1</td>
<td>15</td>
<td>15</td>
</tr>
</tbody>
</table>
2.2.2 Layer characterization

Due to the presence of multi-layers in our III-N samples (buffer layers and active regions), we encountered difficulties to characterize the passivation layer on AlGaN/GaN samples, using only non-destructive techniques such as the ellipsometer, Fourier transform infrared spectroscopy (FTIR) etc... Furthermore, it is insignificant to measure the stress on few cm² samples. For these reasons, SiNx was deposited on both AlGaN/GaN samples and 6 in. Si substrates. Si substrates (6 in. diameter) were then used to measure optically the thickness and to evaluate its uniformity and the refractive index of the as deposited SiNx. Si substrates were also used to measure the bow and consequently to evaluate the possible stress of SiNx layer. FTIR was also conducted on Si substrates in order to analyze the chemical bonds of the layer, mainly, the hydrogen bonds with nitrogen and Si atoms. The characterization of SiNx deposited on Si is meant to give a first approximation. The results may be slightly different when depositing SiNx on large diameter AlGaN/GaN heterostructure.

<table>
<thead>
<tr>
<th>Deposition number</th>
<th>Thickness on Si (nm)</th>
<th>Thickness uniformity (%)</th>
<th>Refractive index n</th>
<th>Stoichiometry x in SiNx</th>
<th>Stress on Si (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN-1</td>
<td>255</td>
<td>2.45</td>
<td>1.936</td>
<td>1.4265</td>
<td>154</td>
</tr>
<tr>
<td>SiN-2</td>
<td>392</td>
<td>4.36</td>
<td>2.053</td>
<td>1.2819</td>
<td>148</td>
</tr>
<tr>
<td>SiN-3</td>
<td>275</td>
<td>4.20</td>
<td>1.937</td>
<td>1.4252</td>
<td>19</td>
</tr>
<tr>
<td>SiN-4</td>
<td>261</td>
<td>0.67</td>
<td>2.024</td>
<td>1.3163</td>
<td>-341</td>
</tr>
<tr>
<td>SiN-5</td>
<td>316</td>
<td>5.70</td>
<td>1.922</td>
<td>1.4449</td>
<td>-129</td>
</tr>
<tr>
<td>SiN-6</td>
<td>352</td>
<td>6.36</td>
<td>1.931</td>
<td>1.4357</td>
<td>40</td>
</tr>
<tr>
<td>SiN-7</td>
<td>301</td>
<td>4.81</td>
<td>1.931</td>
<td>1.4331</td>
<td>-272</td>
</tr>
<tr>
<td>SiN-8</td>
<td>344</td>
<td>6.58</td>
<td>1.949</td>
<td>1.4097</td>
<td>-113</td>
</tr>
<tr>
<td>SiN-9</td>
<td>278</td>
<td>4.58</td>
<td>1.943</td>
<td>1.4174</td>
<td>-368</td>
</tr>
<tr>
<td>SiN-10</td>
<td>334</td>
<td>6.42</td>
<td>1.972</td>
<td>1.3804</td>
<td>-429</td>
</tr>
</tbody>
</table>

First, the ellipsometer was used to measure the thickness and refractive index at different points across the 6 in. Si wafer. These values and the uniformity are reported in Table 2-5. At a gas ratio of 1:3, when the power increases, the thickness increases, while the refractive index and the stress slightly decreases (comparison of SiN-1, 3 and 6). At a gas ratio of 1:1, the effect of the power on the thickness is unclear, especially at 200 W. This can be attributed to the low power that dissociates hardly the species in the plasma. However, when the power increases at this ratio, the refractive index and the stress decreases. Regardless of the power and SiH₄ flow, when the gas ratio increases, the thickness and the stress decrease (comparing SiN-3 to 4, SiN-
5 to 7 and to 9 and SiN-6 to 8 and to 10). Nevertheless, the refractive index increases (comparing SiN-1 to 2, SiN-3 to 4, SiN-5 to 7 and to 9 and SiN-6 to 8 and to 10). At a fixed SiH$_4$ flow, when NH$_3$ increases, the thickness and the stress also increase while the refractive index decreases (comparing SiN-5 to 7 and to 9 and SiN-6 to 8 and to 10). Finally, regardless of NH$_3$ or the total gas flow, the thickness and the refractive index increase with SiH$_4$ flow (comparing SiN-5 to 6, SiN-7 to 8, SiN-9 to 10 and SiN-7 to 10). The effect on the strain is still hard to understand. Hence, the refractive index $n$ of SiN$_x$ layer varied from 1.922 to 2.053. Comparing to the refractive index of the stoichiometric Si$_3$N$_4$ (2.01), 2 layers are Si-rich (SiN-2 and SiN-4) and 8 are N-rich. The composition $x$ of N in SiN$_x$ is calculated using the following formula$^{107}$:

$$n_{SiN_x} = \frac{n_{a-Si} + \frac{3x(2n_{Si_3N_4} - n_{a-Si})}{1+\frac{3}{4}x}}{1+\frac{3}{4}x}$$

Eq. 2.1

where,

$n_{a-Si}$: amorphous Si refractive index (4.2)

$n_{Si_3N_4}$: stoichiometric Si$_3$N$_4$ refractive index (2.01)

$x$: N composition in SiN$_x$

The composition $x$ extracted from Eq. 2.1 is plotted in Fig. 2-4 versus the deposition number. The dotted red line represents the composition of a stoichiometric Si$_3$N$_4$ (1.333). The Si-rich layers have an $x$ lower than 1.333 and the N-rich layers figures in the upper side of the scheme.

**Fig. 2-4. The stoichiometry of the SiN$_x$ layers calculated using Eq. 2.1. The horizontal dotted red line corresponds to the stoichiometric Si$_3$N$_4$.**
Global layer stress was extracted according to Stoney’s equation (Eq. 2.2)\(^{108}\). The results are presented in Fig. 2-5 as function of the deposition number.

\[
\sigma_f = \frac{E_s}{6(1-v_s)} \cdot \frac{t_s^2}{t_f} \cdot \left(\frac{1}{R} - \frac{1}{R_0}\right)
\]

Eq. 2.2

where,

\(R_0\) and \(R (\approx -\frac{D^2}{8B})\): curvature radius before and after deposition, respectively

\(B\) and \(D\): bow and wafer diameter (\(\mu m\)), respectively

\(\sigma_f\): stress of the layer (MPa)

\(E_s\): substrate Young modulus (taken at 160 GPa)

\(v_s\): substrate Poisson coefficient (0.24)

\(t_s\) and \(t_f\): thickness of the substrate and the layer, respectively

![Fig. 2-5. SiN\(_x\) layers stress in MPa calculated using Eq. 2.2. The horizontal dotted black line corresponds to the stress free SiN\(_x\) layer.](image)

As can be seen in Fig. 2-5, the SiN\(_x\) layer can be in tensile or compressive stress depending on the deposition conditions. Layers such as SiN-3 and SiN-6 are very interesting due to the slight tensile stress, measured on 6 in. Si wafer. Furthermore, these two layers are nitrogen rich. In fact, a N-rich passivation layer is preferred over a Si-rich one due to the presence of Si that can contaminates GaN. For this reason, these 2 layers were selected for the Schottky contact study. SiN-10 is also chosen for comparison reasons due to its high compressive stress (-429 MPa).

The SiN\(_x\) layers were annealed in a rapid thermal annealing (RTA) system at 800 °C for 3 min, in order to simulate high temperature contact annealing. Consequently, the molecular vibration modes in the SiN\(_x\) films were characterized by FTIR before and after annealing. FTIR is also
used to monitor hydrogen content in the SiNₓ films. The hydrogen, incorporated during the deposition process, affects the layer properties such as leakage current, etch rate, film structure etc. \(^{109}\). Reducing the hydrogen concentration in the layer may help increasing the device performance. FTIR was conducted on these 3 layers (SiN-3, 6 and 10), before and after annealing, and the results are presented in Fig. 2-6. The full lines correspond to the as-deposited SiNₓ layers and the dotted lines correspond to the annealed SiNₓ layers. Many bonding modes are visible such as Si-N, Si-H and N-H stretching modes at 829 cm\(^{-1}\), 2175 cm\(^{-1}\) and 3444 cm\(^{-1}\), respectively.

![FTIR spectra of PECVD SiN-3, 6 and 10 films on Si. (a) The full spectra scanned between 380 cm\(^{-1}\) and 3900 cm\(^{-1}\), (b) Si-N symmetric, (c) N-H and (d) Si-H bonding modes. The full and dotted lines correspond to the as-deposited and annealed SiNₓ layers, respectively.](image)

For the as-deposited layers, increasing the power from 350 W to 500 W (SiN-3 and 6), the thickness increases resulting in the increase in Si-N asymmetric bonding mode. However, N-H bonding increases while Si-H bonding remains invariant. On the other hand, decreasing the NH\(_3\) flow from 45 sccm to 15 sccm (SiN-6 to 10) resulted in further decrease in the N-H bonding. Nevertheless, Si-H bonding increases slightly.

It is well known that the dissociation of N-H and Si-H bonding can be achieved by annealing \(^{110}\). The FTIR spectra are presented in Fig. 2-6 (dotted lines). SiN-3 and SiN-6

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exhibited the decrease in N-H and Si-H stretching modes upon annealing. However, SiN-10 showed the decreases in N-H stretching mode and the decrease in Si-H one. Nevertheless, Si-N asymmetric mode of all layers increases meaning that Si-N bonding increases.

For the next study, we selected 3 N-rich SiNₓ layers: 2 layers are in slight tensile strain and the third one is in high compressive strain (selected for comparison). In the following experiments, the etch of these SiNₓ layers is discussed.

2.2.3 Wet and dry etching

The first layer deposited on the AlGaN/GaN heterostructure after surface cleaning during the diode process will be the SiNₓ one. This layer has to be etched at specific regions in order to deposit ohmic and Schottky contacts on the semiconductor. According to the literature ²⁰,⁶¹,⁶⁵, the SiNₓ layer can be wet or dry etched. We have studied both techniques and the results are presented below. It is important to mention that, in the following section, the SiNₓ layers are deposited on the AlGaN/GaN samples.

2.2.3.1 Buffered oxide etch (wet etching)

A mixture of hydrofluoric acid (HF) and ammonium fluoride (NH₄F) is known to etch SiNₓ without damaging the GaN layer. This solution is used firstly to etch the SiNₓ layers after deposition (Table 2-4) on the AlGaN/GaN heterostructure. This resulted in an etching rate ranging between 8.5 nm.min⁻¹ and 23 nm.min⁻¹ depending on the deposition conditions. Nevertheless, this mixture has many drawbacks such as inability to etch completely the SiNₓ layer after annealing (for example, after annealing at 500 °C) and high isotropy (lateral etching). Fig. 2-7 is a scanning electron microscopy (SEM) and illustrates the difficulty to etch the annealed SiNₓ layer, regardless of the deposition conditions. Patterned samples were processed using chemical etching of SiN. However, these patterns remained visible at the surface after annealing and etching in the BOE solution even for longer duration than the one used prior to annealing.
This can be explained by the fact that SiNₓ reacts with GaN after high temperature treatments resulting in a thin layer non-etchable in BOE. On the other hand, the lateral etching is also a major issue. As we intend to use very short field plates (2-4 µm), consequently, a high lateral etching rate results in inaccurate field plates length and incorrect electrical results.

**2.2.3.2 Reactive ion etching**

RIE is an alternate solution to avoid the lateral etching and to eliminate the thin layer formed after annealing. The etching conditions of SiNₓ were previously developed in STMicroelectronics. Consequently, in our work, we applied the existing recipes that consists in a LF and RF power of 500 W and 100 W, respectively. CHF₃ (30 sccm) and C₂H₄ (3 sccm) are used as etching gas.

Surface morphologies were monitored by AFM on the samples after SiNₓ etch (3, 6 and 10) and are compared to a GaN reference one (presented in Fig. 2-8). The dislocations are revealed further as can be seen in 2x2 µm² images. However, the roughness remains invariant (before deposition and after etching) and the atomic steps are still visible after etching. Consequently, SiNₓ layers etching by RIE seems efficient, without affecting seriously GaN surface and this process will be used during the diode process.
### 2.3 Ohmic contacts

Depositing a metal on a semiconductor forms a potential barrier at the interface. Under specific conditions, electrons from the semiconductor flow towards the metal, leaving behind a depleted region in the semiconductor. An electric field appears in the depletion region $W$ and reaches the maximum at the interface metal/semiconductor. To avoid lengthy text, the readers interested in the transport mechanisms can refer to reference $112$. The basics of these mechanisms are shortly described in Appendix A.

A good ohmic contact leads to a linear I-V curve with a low resistance value. However, the resistance is not sufficient to conclude on the good ohmic behavior. Other useful parameters to be extracted are the specific contact resistivity ($\rho_C$ in $\Omega \cdot \text{cm}^2$, also known to as specific contact resistance) and the contact resistance $R_C$ in $\Omega \cdot \text{mm}$ (calculated using $\rho_C$). TLM is a technique used to extract these electrical parameters. TLM are also explained in details in Appendix B. Circular-TLM (C-TLM) consisting in circular metallic contacts of a diameter $D$ and distance $d$ from the outer metallic region are used in our study. The parameters extracted and calculated are presented in Appendix B.
2.3.1 Ohmic contact choice on III-N

The choice of the metal for ohmic contact depends on the metal work function \( q\Phi_M \) and the semiconductor electron affinity \( q\chi_S \). Ideally, metal with \( q\Phi_M < q\chi_S \) leads to the best ohmic contact. The metal Fermi level (under which the electrons are accumulated) will be higher than the bottom of the semiconductor conduction band. In this case, the barrier height \( q\Phi_B \) (Eq. A.1 in Appendix A) is negative resulting in resistance-free electron circulation between metal and semiconductor. However, it is difficult to find metals with a work function lower than the electron affinity of any semiconductor used in microelectronics applications. For instance, the electron affinity of GaN at room temperature is 4.1eV. Thus, a metal with a work function slightly higher than 4.1 eV can be a solution. As discussed in Chapter 1, the metals used as ohmic contacts on GaN (or AlGaN) have a higher work function (e.g. 4.33 eV for Ti) than GaN electron affinity. However, a high n type doping level is required to form a good ohmic contact on GaN. In the case of AlGaN/GaN heterostructure used in our case, a high mobility 2DEG is formed at the interface mainly due to the use of undoped layers. Thus, adding dopants to the material reduces the electron mobility. Furthermore, the AlGaN barrier layer has a larger band gap than GaN, consequently, makes the formation of a good ohmic contact difficult. The transport mechanism in the heterostructure is more complex than the one in simple n-type GaN. Nevertheless, forming a good ohmic contact on the undoped heterostructure is still possible (regardless of the doping level).

2.3.1.1 Previous study on n+ GaN

To avoid daunting experiments on the heterostructure, a simple approach has consisted in transferring the previously obtained results during the previous PhDs from GREMAN on GaN. Menard \(^3\) has studied the ohmic contact on bulk GaN using different metal stacks and GaN surface treatments. Al and Ti/Al metal stacks (Au-free) were sputtered on GaN. Adding Au to the process gives rise to integration compatibility problems. In fact, the passivations (SiNx or SiOx) hardly stick on or under the Au layer making the process unreproducible. In these experiments, Ti thickness varied from 20 nm to 150 nm while Al thickness was kept at 200 nm. The metals were annealed in conventional furnace and RTA system at temperatures varying from 300 °C to 850 °C in different ambients. Chemical surface treatments were also investigated from standard clean 1, 2 (SC1 – 2) and Caro’s to HF (different concentrations) or boiling NH₃OH. He concluded on a good quality ohmic contact annealed at 550 °C and using
Ti (70 nm)/Al (200 nm) on GaN cleaned using SC1 – Caro’s – HF. This work was conducted on thick GaN layers epitaxied on both sapphire and Si.

2.3.1.2 Pre-study of Al thickness impact

As mentioned previously, our study is conducted on the AlGaN/GaN heterostructure, where a 2DEG accumulates at the interface. Based on these previous results, we have fixed Ti thickness to 70 nm and varied Al thickness from 150 nm to 250 nm. The main purpose of this pre-study was to adapt Al thickness in the contact as Al is also present in the barrier layer. C-TLM were processed on samples from the epitaxy of supplier C-I (see Table 2-1, without AlGaN recess). Different annealing temperatures (500 °C - 550 °C - 600 °C, 3 min each under Ar, and an annealing named D - combination of 500 °C and 800 °C - that will be explained later on in 2.3.1.3) were tested. Two surface treatments were also tested namely Caro’s – SC1 – HF (called “Clean 1”) and Boiling NH₄OH 10%. The resulting Rc and ρ_C are presented in Fig. 2-9.

First, regarding sample cleaning, “clean 1” surface treatment seems to give better results than NH₄OH (when annealing at 550 °C). Rc is reduced by approximately the half of its value. Consequently, “clean 1” surface treatment was kept. The best results suggest that a thickness of 180 nm of Al gives the best results.

To understand more in detail the effect of “clean 1”, a sample was cleaned in NH₄OH followed by “clean 1” prior to metal deposition and annealing at 550 °C. The resulting Rc and ρ_C are compared to samples treated only using “clean 1” or NH₄OH as shown in Fig. 2-10.
Rc and $\rho_c$ decreases when mixing both cleaning and reaches the lowest values after only “clean 1” surface treatment. Although Rc and $\rho_c$ resulting from “clean 1” are still relatively high, we could conclude on the efficiency of “clean 1” comparing to NH$_4$OH treatment.

![Graph showing the effect of surface treatments on Rc and $\rho_c$.](image)

Fig. 2-10. Surface treatments effect on the electrical characteristics Rc (triangles) and $\rho_c$ (squares), for a fixed Al thickness of 180 nm and annealing at 550 °C for 3 min in Ar. The slight horizontal shift is for clarity reasons.

It is important to mention the surface degradation of this epitaxy (without GaN cap-layer) after “clean 1”. The AFM images represented in Fig. 2-11 show the evolution of the surface morphology of as-grown samples and after Caro’s and “clean 1” surface treatments. The unprotected AlGaN tends to be teared as the temperature decreases after the epitaxy. After 10 min in Caro’s, these tears are broadened further and the surface roughness slightly increases. After “clean 1”, the tears are even larger and the roughness keeps increasing to reach approximately 1 nm.
We do not recognize the effect of such a surface on the ohmic contacts. However, we carried out the ohmic contact optimization on supplier C-I to demonstrate the achievability of a low Rc.

2.3.1.3 Thermal treatments effect

In this part, we investigated more deeply the anneal temperature effect on the ohmic contact. Firstly, the study was conducted on samples from supplier C-I epitaxy. After “clean 1” surface treatment, C-TLM were processed using Ti (70 nm)/Al (180 nm) metal stack on a recess-free surface. Samples were then rapid thermal annealed at different temperatures before electrical characterization. C-TLM annealed at different temperatures from 500 °C to 800 °C and a multi-temperature annealing were processed on recess-free surface. Then, a comparative study on all suppliers was carried.

In the following part, only samples from supplier C-I are discussed.

- Single temperature annealing

The first set of experiments was annealed at temperatures from 500 °C to 850 °C for 3 min in Ar. The linear characteristic of an ohmic contact is readily observed in Fig. 2-12. The C-TLM results presented in Fig. 2-12 are obtained with a metals distance of 12 µm. A clear ohmic
behavior was obtained with different resistances depending on the anneal temperature. The sample annealed at 500 °C (the lowest temperature – light blue in Fig. 2-12) exhibited the lowest resistance for a given metal distance (12 µm in this case). However, it is important to mention that this resistance (extracted from I-V characteristic) does not reflect a low contact resistance or specific resistivity since it is extracted from a single distance between the contacts.

Fig. 2-12. I-V characteristics for Ti/Al ohmic contacts on samples from supplier C-I epitaxy as function of annealing temperature.

$R_c$ and $\rho_c$ versus annealing temperature are illustrated in Fig. 2-13. $R_c$ increases with annealing temperature up to 650 °C and decreases above this temperature to reach 3.99 Ω.mm at 800 °C. Although a linear I-V characteristic was achieved upon annealing at 850 °C, $R_c$ at this temperature is very high, as shown in Fig. 2-13. At this high temperature, we suggest that the out-diffusion of nitrogen from GaN deteriorates the surface and consequently degrades the 2DEG. Similarly to $R_c$, the lowest $\rho_c$ (1x10$^4$ Ω.cm) is obtained upon annealing at 800 °C. It is worth mentioning that although annealing at 500 °C leads to the lowest resistance (at a given TLM distance), the sample showed a relatively high $R_c$ and $\rho_c$ (6.2 Ω.mm and 6.1x10$^4$ Ω.cm, respectively).
Fig. 2-13. Contact resistance $R_c$ (triangles) and specific contact resistivity $\rho_c$ (squares) as function of the annealing temperature for Ti/Al on recess-free AlGaN/GaN heterostructure resulting from C-TLM measurements with a metal distance of 12 µm.

It is known that TiAl$_3$ alloys is formed when annealing Ti/Al metal stack on GaN. Greco et al. 68 have reported on Ti/Al ohmic contacts on AlGaN/GaN annealed at 800 °C for 1 min. They have showed the presence of TiAl$_3$ phase on top of a TiN layer at the interface with AlGaN. Hence, XRD is used to investigate the presence of any eventual metal/AlGaN alloys at different annealing temperatures (from 500 °C to 850 °C) and is presented in Fig. 2-14.

Fig. 2-14. XRD 0-20 scans of reference sample (red line) and samples annealed from 500 °C to 850 °C with a step of 50 °C for 3 min, from bottom to top. The spectra are vertically shifted for clarity reasons.
In our study, low intensity peaks of cubic $\text{Ti}_3\text{AlN}$ (111) (200) (220) and $\text{TiAl}_3$ (111), for samples annealed above 800 °C, are found using XRD. It suggests that these alloys may result in the good ohmic behavior after annealing at 800 °C. Despite the presence of these alloys for sample annealed at 850 °C, the bad electrical results can be attributed to the surface degradation at such high temperature, as previously mentioned. It is important to mention that these results were hardly reproducible on supplier C-I samples.

- **Multi-temperature annealing**

Despite the linear ohmic behavior of I-V characteristics, the resulting $R_c$ is still relatively high and has to be improved. Thus, further investigations are conducted to obtain satisfying $R_c$. From the results previously presented, the lowest resistance and $R_c$ were obtained at 500 °C and 800 °C, respectively. Consequently, we intended to mix both annealing temperatures in order to obtain the best I-V characteristic and lowest $R_c$ and $\rho_c$. This resulted in 4 combinations represented in Fig. 2-15.

![Fig. 2-15. Annealing temperature as function of time during the multi-temperature annealings process (A, B, C and D).](image_url)

In these experiments, we vary the temperature rise (7 °C/s or 70 °C/s) with a temperature combination of 500 °C and 800 °C. Anneal A (dark red line in Fig. 2-15) consisted 7 °C/s temperature rise to 800 °C with a 30 sec plateau followed by a temperature decreases to reach a 3 min plateau at 500 °C. Anneal B (green line in Fig. 2-15) is similar to Anneal A only with reversing the temperatures (500 °C, 3 min followed by 800 °C, 30 sec). Anneal C and D (black
and blue lines in Fig. 2-15, respectively) were identical to A and B, respectively, with a 70 °C/s ramp to reach 800 °C.

The comparison of annealing A to C and B to D shows clearly the effect of the slope (7 °C/s or 70 °C/s) on the electrical results, as represented in Fig. 2-16. For clarity reasons, electrical results from samples annealed at 500 °C for 3 min and 800 °C for 30 sec (with 7 °C/s and 70 °C/s slope) are also presented in Fig. 2-16. Rc and \( \rho_c \) decreases with higher slope. Additionally, comparing A to B shows that an 800 °C annealing before the 500 °C one improves slightly the electrical results. Contrarily, comparing C to D shows the opposite results. Rc is lower when the contact is annealed at 500 °C before 800 °C. These results seem a bit contradictory. Nevertheless, it is important to mention that the lowest Rc and \( \rho_c \) were obtained in this study (1.01 Ω.mm and 1.35x10^{-5} Ω.cm², respectively). Comparing to the literature, Hu et al. \(^{58} \) have reported on Au-free Ti/Al/Ti/TiN ohmic contacts annealed at 550 °C on recessed and recess-free AlGaN/GaN. They have achieved 1.5 and 1.8 Ω.mm median Rc for recessed and recess-free wafers, respectively. In our study, the lowest Rc about 1 Ω.mm on Au-free and recess-free AlGaN/GaN heterostructure using only a bi-layer metal stack remains the best value reported before in the literature.

XRD was also conducted on this set of experiment. The alloys found in 2.3.3.3 – Single temperature annealing – namely the cubic Ti₃AlN (111) (200) (220) and TiAl₃ (111), were also found after Anneal B and D as shown in Fig. 2-17 (green and blue spectra, respectively). However, Anneal B resulted in a Rc with a large deviation from the mean value which can be attributed to the slow ramp of temperature (7 °C/s) or to the sample surface state after “clean 1” (Fig. 2-11 in section 2.3.1.2). The sample holder peak appearing at approximately 44.5 ° for all

![Fig. 2-16. Contact resistance Rc (triangles) and specific contact resistivity \( \rho_c \) (squares) as function of the annealing applied on recess-free AlGaN/GaN. Rc and \( \rho_c \) are horizontally shifted for clarity reasons.](image-url)
samples except the one after anneal D is related to the sample alignment prior to the measurement.

To investigate in details the Anneal D that results in the best ohmic characteristics, a second set of samples was annealed combining 500 °C and 800 °C (Anneal D). The annealing duration at 800 °C was varied from 10 sec to 3 min. $R_c$ and $\rho_c$ are plotted in Fig. 2-18 as function of annealing duration at 800 °C. This resulted in a U-shape scheme, meaning that the optimal conditions have been reached and corresponds to the sample annealed at 500 °C for 3 min followed by 800 °C for 30 sec with a ramp of 70 °C/s (called Anneal D).

![Fig. 2-17. XRD 0-20 scans of reference sample (red line) and samples annealed A (dark red line), B (green line), C (black line) and D (Blue line), from bottom to top, respectively. The spectra are vertically shifted for clarity reasons.](image)

![Fig. 2-18. Contact resistance $R_c$ (triangles) and specific contact resistivity $\rho_c$ (squares) as function of the annealing duration at 800 °C for Ti/Al on recess-free AlGaN/GaN.](image)
As previously mentioned, the good ohmic behavior according to the literature has been attributed to the presence of TiAl$_3$ phase on top of a TiN layer at the interface with AlGaN. In our study, when increasing Al thickness to 240 nm, we observed the presence of tetragonal TiAl$_3$ (00l) peaks. However, at this thickness, Rc increased to reach 3.64 Ω.mm (Fig. 2-9).

To conclude on this first study, we have studied ohmic contacts on samples from supplier C-I using Ti (70 nm)/Al bi-layer. Al thickness was varied from 150 nm to 240 nm. Two surface treatments were investigated ("clean 1” and NH$_4$OH). Contacts were annealed at single temperatures from 500 °C to 850 °C (by step of 50 °C) or at multi-temperatures (Anneal A, B, C and D). The lowest Rc and $\rho_c$ (1.01 Ω.mm and 1.35x$10^{-5}$ Ω.cm$^2$, respectively) corresponds to the sample annealed at 500 °C for 3 min followed by 800 °C for 30 sec with a ramp of 70 °C/s (called Anneal D). However, the exact phenomenon responsible for good ohmicity remains unclear. Even though cubic Ti$_3$AlN and TiAl$_3$ peaks appeared on the XRD spectrum, complementary and lengthy investigations, such as TEM imaging, have to be conducted to understand further the mechanism lying behind this result.

- **Ohmic contacts comparison on all suppliers**

A good ohmic behavior was obtained on supplier C-I using Ti (70 nm)/Al (180 nm) upon anneal D and resulting in a very low Rc of 1 Ω.mm. The reproducibility of such a process on different epitaxy remains a question to be answered and will be discussed in the following section.

The second study consisted in annealing C-TLM processed on samples from different suppliers at different temperatures from 500 °C to 800 °C and a multi-temperature (Anneal D). “Clean 1” surface treatment was used prior to Ti (70 nm)/Al (180 nm) metal sputtering.

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**Fig. 2-19.** Rc and $\rho_c$ as function of the annealing applied on recess-free AlGaN/GaN from all suppliers. The slight horizontal shift is for clarity reasons.
The resulting \( R_c \) and \( \rho_c \) are presented in Fig. 2-19. Without the presence of GaN cap-layer (supplier C-I samples), the I-V characteristics are linear and exhibit an ohmic behavior. The lowest \( R_c \) of 1 \( \Omega \).mm is obtained after Anneal D. Supplier A and supplier C-II epitaxy (with GaN cap-layer) showed linear I-V characteristics after annealing only at 800 \( ^\circ \)C. \( R_c \) is estimated to be 2.94 and 6.5 \( \Omega \).mm, respectively for both samples. This can be explained by the presence of the GaN cap-layer at the surface acting as a dielectric layer. Consequently, the recess of these structures is necessary in order to achieve a low contact resistance. On the other hand, samples from supplier B exhibited linear I-V characteristics with a relatively low \( R_c \) (< 5 \( \Omega \).mm). The lowest \( R_c \) of 1.74 \( \Omega \).mm was obtained after Anneal D. Despite the presence of a GaN cap-layer, the low contact resistance on samples from supplier B can be attributed to the strain in the epilayers as presented in Fig. 2-3. Sample from supplier C-I (without GaN cap-layer) still showed the lowest \( R_c \) of 1 \( \Omega \).mm after anneal D.

### 2.3.1.4 Chemical surface treatments impact

We have demonstrated in section 2.3.1.2 the efficiency of “clean 1” treatment compared to \( \text{NH}_4\text{OH} \) treatment on samples from supplier C-I. In this section, we will compare the effect of both surface treatments on samples from supplier C-I, C-II, A and B. Reference samples seeing only water rinsing (to eliminate particles from the surface) are also processed for comparison. C-TLM are processed using Ti (70 nm)/Al (180 nm) bi-layer metal stack on recess-free epitaxies, undergoing Anneal D. Fig. 2-20 represents electrical results (\( R_c \) and \( \rho_c \)).

![Fig. 2-20. \( R_c \) and \( \rho_c \) characteristics on recess-free AlGaN/GaN from all suppliers as function of the surface treatments applied. The Red color represents \( \text{NH}_4\text{OH} \), the black one represents “clean 1” and the green one represents water rinsing. Resistances of supplier C-II and supplier A are estimated from non-linear I-V measurements. The slight horizontal shift is for clarity reasons.](image-url)

We remind that the epitaxy of supplier C-I is without GaN cap-layer and the one of supplier C-II, A and B have a GaN cap-layer that protects the AlGaN barrier surface. This cap-layer,
consisting in an undoped wide band gap material and mainly not participating to the formation of the 2DEG, can act as a dielectric-like layer. Thus, this cap-layer can be the reason behind the non-linear I-V characteristics of samples from supplier C-II and A. Consequently, the calculated resistances are overvalued. A recess (explained in 2.3.1.5) of GaN/AlGaN/GaN is unavoidable for some structures. On the other hand, samples from supplier B exhibited linear I-V characteristics despite the presence of the cap-layer. As can be seen in Fig. 2-20, “clean 1” exhibited the lowest $R_c$ and $\rho_c$ followed by reference sample. NH$_4$OH surface treatment degraded the electrical characteristic. Consequently, we can conclude on the efficiency of “clean 1” prior to ohmic contact deposition on these samples and the one processed on supplier C-I.

Supplier C is the main supplier in our project (Tours 2015). Despite the good ohmic contact resistance obtained on samples from C-I, the number of wafers dedicated to the study was limited. Furthermore, despite the very bad contact resistance on C-II epitaxy, this epitaxy is the new generation epitaxy, thus, the Schottky diodes are to be processed on samples from supplier C-II. From this section, we conclude the difficulty to transfer the ohmic contact process from an epitaxy to another. Consequently, a detailed study on supplier C-II is mandatory to optimize the ohmic contact, considering that a contact resistance below 3 Ω.mm is acceptable for the diode process.

2.3.1.5 Recessed ohmic contacts

This study is conducted on samples from supplier C-II with a GaN cap-layer on top of AlGaN barrier. Based on the results reported in 2.3.1.3, we attribute the non-linear I-V characteristics to the presence of the GaN cap-layer on top of AlGaN. Consequently, to obtain a good ohmic contact, a recess step of the heterostructure (to remove GaN under the ohmic contact) is unavoidable. As explained previously in Chapter 1, different types of recess are possible: shallow, partial and full recess. The advantage of the first two is the presence of a sufficiently thick AlGaN layer after the recess in order to maintain the 2DEG under the contact. On the other hand, the full recess presents another benefit for the contact. Even though the 2DEG is totally removed under the contact, the latter contacts the 2DEG from the side resulting in an easy carrier transport between the semiconductor (or 2DEG) and the metal.
- **Recess by ion beam etching**

The recess consists in etching few nm to 30 nm of AlGaN/GaN. A passivation (SiNₓ layer) is deposited prior to recess. From the study of SiNₓ layers presented in 2.2, we choose a SiNₓ layer with a low stress (+19 MPa) and a refractive index (1.937) lower than the one of a stoichiometric Si₃N₄ (2.01) resulting in N-rich layer. SiN-3 from Table 2-5 was chosen with a fixed thickness of 100 nm.

SiN-3 was etched by RIE as previously showed. The chemicals used in this step do not etch GaN-based layers (namely, CHF₃ and C₂H₄). Ion beam etching of GaN and AlGaN was conducted with a low etch rate of 2 nm.min⁻¹. This etch rate allowed to control precisely the etched thickness of the layers. Fig. 2-21 shows a cross sectional view of the 3 recesses studied.

![Cross sectional view of recessed C-TLM](image)

**Fig. 2-21.** Cross sectional view of (a) shallow, (b) partial and (c) full recessed C-TLM, from left to right, using 70 nm/180 nm of Ti/Al. The 2DEG appears at the AlGaN/GaN interface.

- **Impact of recess depth and thermal treatments**

The shallow recess eliminates the GaN cap-layer and enables the contact to be located in the barrier layer. The partial recess aims to take contact more deeply in AlGaN while keeping the 2DEG beneath the metals. The full recess contacts the 2DEG by the side. “Clean 1” is used prior to metal deposition on the recessed heterostructure. Samples are annealed from 500 °C to 800 °C and Anneal D and the electrical results are presented bellow (Fig. 2-22).
Fig. 2-22. The resulting $R_c$ and $\rho_c$ using different annealings for (a) shallow recessed samples, (b) partial recessed samples and (c) full recessed samples.

The shallow recess is presented in Fig. 2-22a and shows that only after annealing at 800 °C, $R_c$ is low enough to reach $3 \, \Omega \cdot \text{mm}$. The full recess (Fig. 2-22c) exhibits a low $R_c$ of $4.3 \, \Omega \cdot \text{mm}$ after annealing at 700 °C. However, the partial recess resulted in the lowest $R_c$ of $2.8 \, \Omega \cdot \text{mm}$ (Fig. 2-22b) after annealing at 800 °C. The resulting sheet resistance of $480 \, \Omega / \text{sq}$ is comparable to the one post-epitaxy. This result was verified on 18 different samples and will be used in diode process.

The large study on ohmic contacts led to the following conclusion: a contact resistance of $2.8 \, \Omega \cdot \text{mm}$ and a sheet resistance of $480 \, \Omega / \text{sq}$ were obtained after the partial recess of AlGaN/GaN (14 nm etched) prior to “clean 1” surface treatment and using Ti (70 nm)/Al (180 nm) metal stack annealed at 800 °C for 3 min in Ar. This process is clearly not the best of the one obtained. Nevertheless, they are extremely stable and will hence enable us to process the diodes.
2.4 Schottky contacts

After the study of SiN$_x$ passivation and ohmic contacts, the Schottky contacts are presented in this section of Chapter 2. The Schottky barrier can be calculated as function of the metal work function. Consequently, metals with high work function are preferentially used as Schottky contacts on n-type materials.

2.4.1 Metal choice and pre-study

As discussed in Chapter 1, metals with work function higher than 4.5 eV are potential candidates to form Schottky barriers on the heterostructure. Among these metals, Ni/Au stack is one of the most used according to the literature $^{13,43,57,86–89}$. However, Au is unsuitable for our devices. Au generates passivation sticking problem (on or under Au). Menard $^3$ has also studied Schottky contacts on GaN. He has used sputtered Ni as a Schottky contact on n-type GaN with varied thickness (20 nm to 500 nm) and annealed at different temperatures from 400 °C to 550 °C. He has found an optimal Schottky contact using 300 nm of Ni annealed at 400 °C for 3 min in N$_2$. This result was hence used as starting point for this study.

2.4.2 Schottky to Schottky structures

Based on this result, we have also chosen a 300 nm thick Ni layer as a Schottky contact. Schottky to Schottky (S2S) structures were firstly used to study the effect of different parameters on the Schottky contact. These structures help studying the Schottky contact independently from other technological steps with a single photolithography level. They also give a first approximation of $q\Phi_B$ without having to process a whole diode (see $^7$).

Fig. 2-23. Schottky to Schottky structures (a) cross sectional and (b) top view.

S2S structures consist in two identical metal contacts where the first block is encircling the second one. The distance is constant while the surface of the contacts varies. The C-shaped
contact (outside contact) surface varies from $3 \times 10^{-3}$ to $10^{-2}$ cm$^2$ while the center contact surface varies from $3 \times 10^{-4}$ to $10^{-3}$ cm$^2$. Fig. 2-23 shows a cross sectional view and a top view of a S2S structure, from left to right, respectively. Based on the fact that Ni forms a Schottky barrier on the heterostructure, when applying a bias, the current flows in the first contact (forward biased). However, the second one blocks the current. At a given bias, we compare the current density and conclude on different treatments used.

### 2.4.2.1 Anneal temperature effect

The first set of experiments was conducted on samples from supplier C-I epitaxy (see Table 2-1). The anneal temperature varied from 350 °C to 550 °C for 3 min in Ar. Fig. 2-24a and b show respectively the current density as function of the applied bias and for a given bias (50 V and 200 V) as function of the annealing temperature. The leakage current $J$ increases with the temperature. For low temperature annealings, $J$ increases slightly. However, for higher temperature (> 500 °C), $J$ increases by one order of magnitude. Although the anneal temperatures 350 °C and 400 °C exhibited similar values of $J$, the lowest thermal budget was chosen. Hence, we kept the 350 °C anneal temperature and varied the time and the atmosphere.

![Graph showing current density vs. anneal temperature](image)

**Fig. 2-24.** (a) Current density-voltage characteristics of S2S structure for different anneal temperatures and (b) current densities at 50 V (red squares) and 200 V (blue circles) as function of the annealings.

In the second set of samples, the anneal temperature is fixed to 350 °C for 1 or 3 min under Ar or N$_2$. From Fig. 2-25 we conclude that annealing for 1 min is more efficient than the 3 min one, regardless of the atmosphere used. However, one can see a clear advantage of N$_2$ annealing atmosphere comparing to Ar.
Scanning transmission electron microscopy (STEM) was done on samples annealed the lowest and the highest temperatures in order to understand further the electrical results and are presented in Fig. 2-26. The annealings were processed under Ar to avoid nitrogen contamination. A reference sample is also presented for comparison (Fig. 2-26a). The uniformity of the AlGaN barrier thickness is influenced by the presence of defects as shown in Fig. 2-26a. Greco et al. 68 have reported the presence of V-shaped defects at the heterostructure surface. They have reported that these V-shaped defects are well-oriented following the (11-20) direction and equivalent and also forms a 43° with the (0001) surface. The Ni deposited at the surface and annealed tend to fill these defects resulting in Ni-rich zones closer to the 2DEG.
Fig. 2-26. STEM cross-sectional view of (a) a reference sample heterointerface, (b) Ni/AlGaN/GaN interfaces annealed at 350 °C for 3 min in Ar and (c) Ni/AlGaN/GaN interfaces annealed at 550 °C for 3 min in Ar.

To identify the atomic composition at different zones, energy-dispersive X-ray spectroscopy (EDS) is performed on both samples. Fig. 2-27 and Fig. 2-28 show STEM cross section of the GaN/AlGaN/metal interfaces from left to right for the sample annealed at 350 °C and 550 °C, respectively. Table 2-6 and Table 2-7 summarize the EDS results of Ga, N, Al, Ni and the contaminants for the sample annealed at 350 °C and 550 °C, respectively.
Fig. 2-27. STEM cross section image of the GaN/AlGaN/metal interface after annealing at 350 °C for 3 min in Ar.

Table 2-6. EDS data of the points from the sample annealed at 350 °C for 3 min in Ar. The points numbering corresponds to the one in Fig. 2-27.

<table>
<thead>
<tr>
<th>Points</th>
<th>Ga (%)</th>
<th>N (%)</th>
<th>Al (%)</th>
<th>Ni (%)</th>
<th>Contaminants (C, O…) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Point 1</td>
<td>67</td>
<td>21.4</td>
<td>0.6</td>
<td>0.5</td>
<td>14.5</td>
</tr>
<tr>
<td>Point 2</td>
<td>64</td>
<td>20</td>
<td>0.5</td>
<td>0.5</td>
<td>15</td>
</tr>
<tr>
<td>Point 3</td>
<td>51</td>
<td>27</td>
<td>6.6</td>
<td>0.6</td>
<td>14.8</td>
</tr>
<tr>
<td>Point 4</td>
<td>20</td>
<td>8</td>
<td>4</td>
<td>44</td>
<td>24</td>
</tr>
<tr>
<td>Point 5</td>
<td>38</td>
<td>17</td>
<td>6.5</td>
<td>19</td>
<td>19.5</td>
</tr>
<tr>
<td>Point 6</td>
<td>25</td>
<td>5</td>
<td>5</td>
<td>42</td>
<td>23</td>
</tr>
<tr>
<td>Point 7</td>
<td>1.5</td>
<td>0</td>
<td>1</td>
<td>75</td>
<td>22.5</td>
</tr>
<tr>
<td>Point 8</td>
<td>1.3</td>
<td>0</td>
<td>1</td>
<td>77</td>
<td>20.7</td>
</tr>
</tbody>
</table>
Fig. 2-28. STEM cross section image of the GaN/AlGaN/metal interface after annealing at 550 °C for 3 min in Ar.

Table 2-7. EDS data of the points from the sample annealed at 550 °C for 3min in Ar. The points numbering corresponds to the one in Fig. 2-28.

<table>
<thead>
<tr>
<th>Points</th>
<th>Ga (%)</th>
<th>N (%)</th>
<th>Al (%)</th>
<th>Ni (%)</th>
<th>Contaminants (C, O…) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Point 1</td>
<td>36.5</td>
<td>17.5</td>
<td>0.3</td>
<td>0.2</td>
<td>45.5</td>
</tr>
<tr>
<td>Point 2</td>
<td>30</td>
<td>20</td>
<td>3</td>
<td>0.3</td>
<td>46.7</td>
</tr>
<tr>
<td>Point 3</td>
<td>16</td>
<td>13</td>
<td>1.8</td>
<td>13.5</td>
<td>55.7</td>
</tr>
<tr>
<td>Point 4</td>
<td>9</td>
<td>10</td>
<td>1.3</td>
<td>22</td>
<td>57.7</td>
</tr>
<tr>
<td>Point 5</td>
<td>7.2</td>
<td>10</td>
<td>1</td>
<td>21</td>
<td>60.8</td>
</tr>
<tr>
<td>Point 6</td>
<td>7</td>
<td>7</td>
<td>0.2</td>
<td>30</td>
<td>55.8</td>
</tr>
<tr>
<td>Point 7</td>
<td>0.5</td>
<td>5</td>
<td>0</td>
<td>30</td>
<td>64.5</td>
</tr>
<tr>
<td>Point 8</td>
<td>0.3</td>
<td>7</td>
<td>0.2</td>
<td>30</td>
<td>62.5</td>
</tr>
</tbody>
</table>

Both samples exhibited Ni-rich zones at the interface with AlGaN and the presence of Ni in the defects at the AlGaN barrier surface confirming the previous conclusion (Fig. 2-26). For the sample annealed at 350 °C, the presence of nitrogen was not detected in the metal layer. However, NiNₓ alloy was found in the metal layer of the sample annealed at 550 °C showing that even at this relatively low temperature, the nitrogen exo-diffuses from the AlGaN/GaN heterostructure towards the Ni layer.
2.4.2.2 Recess effect

For the following experiment, we have chosen 300 nm of Ni annealed at 350 °C for 3 min in N₂. The structure used previously does not include a passivation layer between the contacts. However, in the following experiments, a passivation layer (100 nm of SiN-3) is used.

Samples from supplier C-II epitaxy (with GaN cap-layer) are used to study the effect of the recess on the Schottky contact. S2S are processed on samples without the removal of GaN cap-layer (Fig. 2-29a), with 4 nm of recess (shallow recess, Fig. 2-29b) and with 30 nm of recess (full recess, Fig. 2-29c). Samples were annealed at 350 °C for 3 min in N₂.

Fig. 2-29. Cross sectional view of (a) recess-free, (b) shallow and (c) full recessed S2S structures, from left to right, using 300 nm of Ni. The 2DEG appears at the AlGaN/GaN interface.

As previously, the current density as function of the bias is plotted in Fig. 2-30. The shallow recess results in the lowest leakage current density at any bias. This part helped to fix the recess in order to study the annealing temperature and the passivation effect on the leakage current in section 2.4.2.3.

Fig. 2-30. Current density-voltage characteristics of S2S structure annealed at 350 °C for 3 min in N₂ as function of the recess applied.
2.4.2.3 Passivation choice

The passivation layer is used to isolate the device. It can be also used to protect the semiconductor during thermal treatments or implantation. In this study, samples were passivated with 3 different layers (SiN-3 – 6 – 10 from Table 2-4) of 100 nm thick each and annealed at different temperature from 350 °C to 550 °C for 3 min in N$_2$ while fixing the recess (shallow recess in Fig. 2-31a).

![Diagram](image)

**Fig. 2-31.** (a) Shallow recessed S2S structure using different SiN$_x$ layers and (b) current densities at 50 V (red squares) and 200 V (blue circles) as function of the annealing applied and the SiN$_x$ layer used.

We found that when SiN$_x$ layer is in compression (SiN-10), the leakage current density at 50 V is relatively high (between 1.5 and 4.5x10$^{-4}$ A.cm$^{-2}$) regardless of the anneal temperature of the contact. On the other hand, SiN$_x$ layers in tensile stress (SiN-3 and 6) showed temperature dependent current densities. Annealing above 450 °C resulted in high J (> 6.5x10$^{-4}$ A.cm$^{-2}$). However, low current densities about 1x10$^{-5}$ A.cm$^{-2}$ are obtained after annealing at 350 °C. These results led to fix the passivation layer for the diodes process presented later on.

2.5 Conclusions

In this chapter, we have presented the different heterostructures from different suppliers used in our study and the surface and structural characterizations. Secondly, the SiN$_x$ passivation used in GaN-based devices has been studied. The characterizations have showed that SiN$_x$ layers can be Si-rich or N-rich layers with a refractive index higher or lower to the one of stoichiometric Si$_3$N$_4$ (2.01). We have also found that the layers can be in compressive or tensile stress depending on the deposition conditions.
The third part has dealt with ohmic contacts. The main objective was to obtain Au-free ohmic contacts with a low contact resistance (lower than $3 \, \Omega \cdot \text{mm}$). This objective can be achieved by using an adequate surface treatment and, in some cases, the good recess depth. In our first study on AlGaN/GaN heterostructures without GaN cap-layer, we have found that annealing at 2 different temperatures (anneal D) resulted in a very low contact resistance of $1 \, \Omega \cdot \text{mm}$ on Au-free and recess-free heterostructure. This result has never been reported before in the literature. However, we have found a low contact resistance ($2.8 \, \Omega \cdot \text{mm}$) on different heterostructures using Ti (70 nm)/Al (180 nm) ohmic contacts on a 14 nm recessed structure and annealed at $800 \, ^\circ \text{C}$ for 3 min in Ar. The specific contact resistivity and the sheet resistance were about $1.7 \times 10^{-4} \, \Omega \cdot \text{cm}^2$ and $480 \, \Omega / \text{sq}$, respectively.

As for last study on the Schottky contact, we have found that a combination of annealing-recess-passivation is needed to obtain a low leakage current at high bias. The best result has been achieved using a 300 nm Ni contact on 4 nm recessed AlGaN and annealed at $350 \, ^\circ \text{C}$ for 3 min in N$_2$.

The results in this chapter are essential to the diode process since all the diode components are studied and fixed, mainly the ohmic and Schottky contacts (recess, annealing and surface treatments) and the passivation layer.
Chapter 3. Fabrication and characterization of Schottky barrier diodes
In Chapter 2, we have showed different technological steps to process a Schottky barrier diode (SBD). A SiN$_x$ passivation layer study was presented followed by the ohmic contacts (cathode) on recessed and recess-free structures. Finally, the Schottky contact (anode) was chosen based on Schottky to Schottky structures. This chapter is dedicated to the fabrication and the characterization of a complete high power SBD on the AlGaN/GaN heterostructure, combining the technological steps previously mentioned.

In the first section, we show the detailed fabrication process of the SBD, from the device isolation to the contact annealings. Then, we describe the used mask and the processed SBD. The last section deals with their electrical characterizations. The forward characteristics leads to parameters extraction such as the Schottky barrier height etc…, while the reverse bias gives information about the leakage current and the breakdown voltage. Finally, we compare our study with the state of the art, extracted from the literature and present design optimization perspectives with regard to the literature.
3.1 Diodes fabrication process

SBD process is presented in this section. The device fabrication procedure required up to 6 photolithography steps. A cross section schematics of a single SBD process flow is shown in Fig. 3-1. The 14 steps SBD process is described in the next sections.

3.1.1 Devices isolation and first passivation

After initial surface cleaning (“clean 1”: Caro’s – standard clean 1 - HF) – step 1 in Fig. 3-1, a 100 nm thick SiN-3 layer was deposited on the samples and etched by RIE using a photoresist mask (step 2). Prior to device isolation, the partial recess of the ohmic contact (consisting in etching 14 nm of AlGaN) was performed by IBE (step 3). Later on, device electrical isolation was performed by Ar ion implantation at 230 keV (step 4). A positive photoresist on top of the SiN₃ was used as a hard mask to prevent Ar penetration in undesired zones.

3.1.2 Ohmic contact and second passivation

Prior to Ti (70 nm)/Al (180 nm) metal deposition, “clean 1” was used again to remove the remaining photoresist, organic and metallic contaminations from the surface (step 5). Afterwards, Ti/Al layers were etched by RIE using Cl₂ and BCl₃ (step 6). The photoresist was removed in oxygen plasma. The samples were then annealed at 800 ºC for 3 min (step 7). To verify the electrical results previously reported in Chapter 2, one C-TLM from each sample was electrically measured.

3.1.3 Schottky contact

Once it has been verified that the ohmic contacts were satisfactory, a 150 nm thick SiN-3 layer was deposited on the surface (step 8). Both SiN₃ layers were etched by RIE using the adequate mask (step 9). The anode recess was processed using IBE (step 10) at three different etch depths (shallow, partial and full recess). A 300 nm thick Ni layer was sputtered after surface cleaning (step 11). The samples were cleaned using “clean 1” prior to Ni deposition. The Ni layer was patterned and ion beam etched (step 12) before annealing between 350 ºC – 500 ºC (by 50 ºC step) for 3 min under N₂.

The SiN₃ layer on top of the ohmic contact was etched in HF solution (step 13). The last photolithography step consisted in depositing a photoresist layer between the contacts to avoid
arcing when applying high voltages (step 14). Furthermore, the photoresist is hardened at 180 °C for 30 sec.

Fig. 3-1. Cross section schematics of the process flow described in section 3.1.
3.2 Mask description and varied parameters

The fabrication process requires 6 mask levels that led to the fabrication of SBDs. Circular SBDs with different field plate (FP) length on the anode and the cathode and anode-cathode distance ($L_{AC}$) were subject to the electrical characterization. These circular SBDs of each sample are summarized in Table 3-1.

Table 3-1. Circular SBDs names with the corresponding $L_{AC}$ and FP distance.

<table>
<thead>
<tr>
<th>Diode</th>
<th>$L_{AC}$</th>
<th>Field plates (FP) length</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>15 µm</td>
<td>4 µm</td>
</tr>
<tr>
<td>C2</td>
<td>20 µm</td>
<td>4 µm</td>
</tr>
<tr>
<td>C3</td>
<td>25 µm</td>
<td>4 µm</td>
</tr>
<tr>
<td>C4</td>
<td>15 µm</td>
<td>2 µm</td>
</tr>
<tr>
<td>C5</td>
<td>20 µm</td>
<td>2 µm</td>
</tr>
<tr>
<td>C6</td>
<td>25 µm</td>
<td>2 µm</td>
</tr>
</tbody>
</table>

The field plate structure, which requires no additional process step, is compatible with the fabrication process of conventional HEMTs. For the mentioned reasons, field plates were structured on both ohmic and Schottky contacts as indicated in Fig. 3-1 (step 7 and 12). Field plates on the ohmic contact can reduce the current collapse \(^{28}\). FP is for the protection of the device. However, our devices protection can be improved, and hence, our FP protection is not the optimal.

A top view schematic of a circular SBD (without passivation) is presented in Fig. 3-2a. The perimeter of the Schottky active region is about 942.5 µm. To compare with literature, the current density is expressed in A.mm\(^{-1}\), resulting from the current over the perimeter. As generally done for such devices, the Schottky active region is represented by the contact between the Ni and the AlGaN/GaN and shown in Fig. 3-2b (without the field plates).
Fig. 3-2. (a) Top view schematic of the active regions of a circular SBD, the passivations are not presented. (b) Cross-section schematic of the circular SBD showing the Schottky active region diameter.

The Schottky to Schottky structures (section 2.4.2) resulted in the general conclusion on the contact annealing temperature (annealing under N\textsubscript{2} for 3 min and using SiN-3 passivation layer). However, such structures do not result in an accurate barrier height evaluation and cannot show any forward characteristics. Consequently, SBD were processed combining all the technological steps presented in Chapter 2. The effect of the Schottky recess depth and the annealing temperature of the Ni are studied also in this chapter. A combination of 3 different recesses (shallow, partial and full) and 4 annealing temperatures (350 °C – 500 °C for 3 min in N\textsubscript{2}) is presented in Table 3-2.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anneal temperature (°C)</td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
</tbody>
</table>

### 3.3 Electrical characterization

GaN power devices are mostly used for switching applications where high forward current and high reverse voltage are needed. A compromise must be found between the on-state voltage and resistance and the reverse current (low V\textsubscript{ON}, R\textsubscript{ON} and leakage current). This section is dedicated to the electrical measurements in the forward and the reverse bias.
3.3.1 Forward bias

After processing the Schottky diodes, the forward I-V characteristic is used to calculate the Schottky barrier height and the ideality factor (Fig. 3-3a). The turn-on voltage and the on-state resistance are also extracted from the forward characteristic as shown in Fig. 3-3b.

\[ q \Phi_B = \frac{k_B T}{q} \ln \left( \frac{A^* T^2}{J_s} \right) \]  
Eq. 4.1

where,
- \( k_B \), Boltzmann constant: \( 1.38 \times 10^{-23} \) J.K\(^{-1}\)
- \( T \), temperature (K)
- \( q \), electron charge: \( 1.6.10^{-19} \) C
- \( J_s \), saturation current density (A.mm\(^{-2}\))
- \( A^* \), (theoretical) Richardson constant = \( \frac{4 \pi q m^* k_B^2}{h^3} = 0.26438 \) A.mm\(^{-2}\).k\(^{-2}\)
- \( h \), Planck constant: \( 6.63 \times 10^{-34} \) m\(^2\).kg.s\(^{-1}\)
- \( m^* \), effective electron mass in the crystal

The ideality factor \( n \) is extracted from the following equation:

\[ n = \frac{q}{k_B T} \cdot \frac{1}{\text{slope}} \]  
Eq. 4.2

Fig. 3-3b shows the extraction of the on-state resistance \( R_{\text{ON}} \) and voltage \( V_{\text{ON}} \). Reversing the slope of the line between 1.3 V and 2 V gives the on-state resistance (expressed in \( \Omega \)). Consequently, multiplying the slope reverse with the Schottky contact perimeter and the anode-
cathode distance results in $R_{ON}$, expressed in $\text{m} \Omega \cdot \text{cm}^2$. The intersection of this line with the x-axis gives $V_{ON}$.

### 3.3.1.1 Barrier height and ideality factor

Fig. 3-4 shows the current density (in logarithmic scale) versus the voltage applied as function of the anneal temperature and the recess applied. Fig. 3-4a, b, c and d are representative of the samples annealed at 350 °C, 400 °C, 450 °C and 500 °C, respectively. In each figure, the orange full line is representative of the shallow recessed samples, while the blue and grey full lines are representative of the partially and full recessed samples, respectively. The measurements plotted are the median values of C1 diodes (anode-cathode distance of 15 $\mu$m with a 4 $\mu$m FP). Fig. 3-4 is representative of all the SBDs from the same sample (regardless of $L_{AC}$ and FP length) for the current densities values corresponding to voltages below 0.6 V.

Some samples present a double barrier which can be attributed to the presence of an inhomogeneous layer at the interface metal/semiconductor. As an example, the AlGaN native oxide at the interface may result in a double barrier with the Ni Schottky contact. However, the
double barrier is rarely depicted in the literature as it is not desired in the application and as it is difficult to obtain a clear physical mechanism in the case of a double barrier. Furthermore, SBD with a double barrier generally present a high leakage current in the reverse mode (presented in 3.3.2.1), and hence are unsuitable for power devices. To understand further the mechanism, complementary and lengthy investigations have to be conducted. The presence of a double barrier in some cases (i.e. 400 °C – 4 nm) results in an overestimated barrier height and a low ideality factor, consequently, in inaccurate values.

The first approximation of the barrier height and the ideality factor was based on room temperature measurements. The values reported in Table 3-3 and Table 3-4 are the median values of a minimum of 50 SBDs with the exception of the shallow recessed anode annealed at 350 °C. The barrier height and the ideality factor of the later sample were extracted from about 25 SBDs due to process problems.

Table 3-3 presents the median barrier height, the standard deviation and the highest barrier as a function of the anode recess applied and of the corresponding anneal temperature.

Table 3-3. The median barrier height, the standard deviation and the highest barrier as function of the anode recess applied and the corresponding anneal temperature.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anneal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>temperature</td>
<td>350 400 450 500</td>
<td>350 400 450 500</td>
<td>350 400 450 500</td>
</tr>
<tr>
<td>(°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrier</td>
<td>0.65 0.89 0.71 0.67</td>
<td>0.85 0.7 0.67 0.77</td>
<td>0.88 0.89 0.85 0.83</td>
</tr>
<tr>
<td>height (eV)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Highest</td>
<td>0.68 0.92 0.72 0.69</td>
<td>0.86 0.74 0.68 0.8</td>
<td>0.91 0.91 0.85 0.84</td>
</tr>
<tr>
<td>barrier</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>height (eV)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 3-5 plots the barrier height versus the anneal temperature and the recess applied.
The shallow recessed samples annealed at 350 °C, 450 °C and 500 °C exhibit low barrier heights. However, the sample annealed at 400 °C exhibit a barrier height of 0.89 eV, due to a double barrier. The partial recess exhibit scattered barrier height values, depending on the temperature applied. In this case, the highest barrier of 0.85 eV is obtained upon annealing at 350 °C. Full recessing the anode results in the highest barrier heights at any given temperature. The full recess always gives the best results and the process window seems larger.

Table 3-4 presents the median ideality factor, the standard deviation and the lowest ideality factor as function of the applied anode recess and the corresponding anneal temperature, while Fig. 3-6 plots the ideality factor n versus the anneal temperature and the applied recess.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anneal temperature (°C)</td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
<tr>
<td>Idenity factor n</td>
<td>3.48</td>
<td>2.11</td>
<td>2.34</td>
</tr>
<tr>
<td>Lowest n</td>
<td>3.1</td>
<td>1.88</td>
<td>2.31</td>
</tr>
</tbody>
</table>
After annealing at $350 \, ^\circ C$ and $500 \, ^\circ C$, the ideality factor decreases when the recess depth increases (shallow to partial and full recess), as presented in Fig. 3-6. After annealing at $400 \, ^\circ C$ and $450 \, ^\circ C$, the ideality factor increases when increasing the recess depth from $4 \, nm$ (shallow recess) to $15 \, nm$ (partial recess) and decreases after recessing $30 \, nm$ (full recess).

Once again, the full recessed structures show the lowest ideality factor. An ideality factor higher than 2 means that the current is dominated by generation-recombination phenomenon rather than the thermionic emission. Annealing at $400 \, ^\circ C$ results in the lowest ideality factor of 1.49 and the highest barrier height of 0.89 eV.

Table 3-5 shows Schottky diodes barrier height and ideality factor extracted from the literature and compared to the best result from our study.

Fig. 3-6. The ideality factor versus the anneal temperature and the recess applied. Above the dotted line, the generation-recombination phenomenon dominates the current.
Table 3-5. Schottky diodes barrier height and ideality factor extracted from the literature and our study.

<table>
<thead>
<tr>
<th>Schottky metal</th>
<th>Diode type</th>
<th>Barrier height (eV)</th>
<th>Ideality factor n</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>-</td>
<td>1.13</td>
<td>Between 1.38 and 1.82</td>
<td>13</td>
</tr>
<tr>
<td>TiN/Ti/Al/Ti/TiN</td>
<td>Conventional (similar to our study)</td>
<td>0.55</td>
<td>1.71</td>
<td>70</td>
</tr>
<tr>
<td>Pt/Ti/Au</td>
<td>Planar</td>
<td>0.97</td>
<td>1.67</td>
<td>84</td>
</tr>
<tr>
<td></td>
<td>Recessed</td>
<td>0.62</td>
<td>1.40</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>Recessed</td>
<td>-</td>
<td>1.2</td>
<td>63</td>
</tr>
<tr>
<td>Ni/Au</td>
<td>Planar</td>
<td>0.99</td>
<td>1.29</td>
<td>113</td>
</tr>
<tr>
<td>Ni/Au</td>
<td>Planar</td>
<td>0.8</td>
<td>-</td>
<td>114</td>
</tr>
<tr>
<td>Ni</td>
<td>Recessed</td>
<td>0.89</td>
<td>1.49</td>
<td>Our study</td>
</tr>
</tbody>
</table>

In ref. 13 a barrier height of 1.13 eV and an ideality factor between 1.38 and 1.82 using a Ni layer as a Schottky contact were reported, while a barrier height of 0.55 eV and an ideality factor of 1.71 on conventional diodes (similar to our study) using TiN/Ti/Al/Ti/TiN metal stack as a Schottky contact were reported in ref. 70 and an ideality factor of 1.67 to 1.40 and a Schottky barrier height of 0.97 eV to 0.62 eV for planar and recessed diodes, respectively, using Pt/Ti/Au as an anode contact were reported in ref. 84. These references show a low ideality factor corresponding to a low barrier height. In our study, we report a 1.49 ideality factor corresponding to a 0.89 eV barrier height (best case), considered as high on the undoped AlGaN/GaN heterostructure. An ideality factor of 1.49, as it is the case in our study, is more than an acceptable result. Furthermore, optimizing the SBD design can lead to an improvement in the ideality factor.

3.3.1.2 On-state voltage and resistance

The current density plot versus the voltage applied results in the linear current-voltage characteristic presented in Fig. 3-3b. The ON-state resistance $R_{ON}$ and the turn-on voltage $V_{ON}$ are extracted from the graph as shown in Fig. 3-3b.
• **On-state voltage**

Fig. 3-7 shows the median value of $V_{ON}$ as a function of annealing temperature and the recess depth. $L_{AC}$ and FP length are 15 µm and 4 µm, respectively. The tendency in Fig. 3-7 is similar for each sample regardless of $L_{AC}$ and FP length.

![Graph showing $V_{ON}$ versus anneal temperature and recess depth](image)

**Fig. 3-7.** $V_{ON}$ versus the anneal temperature and the recess applied. The distance $L_{AC}$ and the FP length are 15 µm and 4 µm, respectively (C1 diodes).

In order to present a simplified analysis, the samples will be classified in different groups depending on the process parameters.

From Fig. 3-7, we can notice that upon annealing at 400 ºC and 500 ºC, $V_{ON}$ decreases when the recess depth increases. After annealing at 350 ºC and 450 ºC, $V_{ON}$ increases when the recess depth increases (only from shallow to partial recess) and decreases after the full recess.

However, for shallow recess, $V_{ON}$ increases by 0.2 V when the temperature increases from 350 ºC to 400 ºC, and decreases to reach 0.76 V and 0.72 V after annealing at 450 ºC and 500 ºC, respectively. For the partial, $V_{ON}$ decreases when the temperature increases. As for the full recess, $V_{ON}$ is practically invariant for the samples annealed at 350 ºC, 400 ºC and 450 ºC. $V_{ON}$ decreases slightly to reach the lowest values in our study after annealing at 500 ºC.
At a given anneal temperature, the lowest $V_{\text{ON}}$ is achieved after full recess. In this case (full recess), $V_{\text{ON}}$ varies between 0.64 V and 0.73 V depending on the temperature. In fact, the recess brings the anode closer to or in contact with the 2DEG, and consequently, reduces $V_{\text{ON}}$.

From Fig. 3-7, we can also notice that $V_{\text{ON}}$ is significantly reduced after annealing at 500 °C, for any recess applied, meaning that the high temperature annealing helps diffusing the metal into the AlGaN layer (in the case of shallow and partial recess) resulting in a low $V_{\text{ON}}$. However, the main inconvenient of the later cases (shallow and partial recess annealed at 500 °C) is the high ideality factor and the low barrier height (see Fig. 3-5 and Fig. 3-6). Consequently, this may result in higher leakage current (discussed in section 3.3.2.1).

It is important to mention that the previous paragraph discussed only $V_{\text{ON}}$ of C1 diodes ($L_{\text{AC}}$ and FP length are 15 µm and 4 µm, respectively) presented in Fig. 3-7. However, as previously mentioned, the same tendencies are observed on the other diodes, namely C2 ($L_{\text{AC}}$ of 20 µm and FP length of 4 µm), C3 ($L_{\text{AC}}$ of 25 µm and FP length of 4 µm), C4 ($L_{\text{AC}}$ of 15 µm and FP length of 2 µm), C5 ($L_{\text{AC}}$ of 20 µm and FP length of 2 µm) and C6 ($L_{\text{AC}}$ of 25 µm and FP length of 2 µm). Table 3-6 summarizes $V_{\text{ON}}$ of each sample for all the diodes.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
<tr>
<td>$V_{\text{ON}}$ (V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>0.91</td>
<td>0.76</td>
<td>0.72</td>
</tr>
<tr>
<td>C2</td>
<td>0.9</td>
<td>0.74</td>
<td>0.7</td>
</tr>
<tr>
<td>C3</td>
<td>0.8</td>
<td>0.74</td>
<td>0.7</td>
</tr>
<tr>
<td>C4</td>
<td>0.93</td>
<td>0.76</td>
<td>0.74</td>
</tr>
<tr>
<td>C5</td>
<td>0.91</td>
<td>0.75</td>
<td>0.72</td>
</tr>
<tr>
<td>C6</td>
<td>0.95</td>
<td>0.74</td>
<td>0.71</td>
</tr>
</tbody>
</table>

The full recess, at any anneal temperature, shows the most interesting $V_{\text{ON}}$. This can be attributed to closeness between the anode and the 2DEG. However, in this case, $V_{\text{ON}}$ variation depending on $L_{\text{AC}}$ is practically negligible, for a given FP length, as shown in Fig. 3-8. One can
also notice from Fig. 3-8 that $V_{\text{ON}}$ decreases when the FP length increases from 2 µm (Fig. 3-8b) to 4 µm (Fig. 3-8a).

Fig. 3-8. $V_{\text{ON}}$ versus the anneal temperature for the full recessed samples. Three $L_{\text{AC}}$ distances (15 µm, 20 µm and 25 µm) are presented for (a) a FP length 4 µm and (b) a FP length of 2 µm, respectively. The spectra are horizontally shifted for clarity reasons.

- **On-state resistance**

Fig. 3-9 shows the median $R_{\text{ON}}$ versus the anneal temperature and the recess applied for diodes with (a) $L_{\text{AC}}$ of 15 µm (C1) to 20 µm (C2) and 25 µm (C3) and FP length of 4 µm and (b) $L_{\text{AC}}$ of 15 µm (C4) to 20 µm (C5) and 25 µm (C6) and FP length of 2 µm.
Fig. 3-9. $R_{ON}$ versus the anneal temperature and the recess applied for diodes with (a) $L_{AC}$ of 15 µm (C1), 20 µm (C2) and 25 µm (C3) and FP length of 4 µm and (b) $L_{AC}$ of 15 µm (C4), 20 µm (C5) and 25 µm (C6) and FP length of 2 µm.
Table 3-7 summarizes \( R_{\text{ON}} \) of each sample as a function of \( L_{\text{AC}} \) and FP length.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annel temperature (^{\circ}\text{C})</td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
<tr>
<td>( R_{\text{ON}} ) (m(\Omega).cm(^2))</td>
<td>C1 2.12</td>
<td>2.77</td>
<td>1.73</td>
</tr>
<tr>
<td></td>
<td>C2 3.24</td>
<td>4.03</td>
<td>2.92</td>
</tr>
<tr>
<td></td>
<td>C3 6.04</td>
<td>6.2</td>
<td>4.13</td>
</tr>
<tr>
<td></td>
<td>C4 1.56</td>
<td>2.71</td>
<td>1.72</td>
</tr>
<tr>
<td></td>
<td>C5 3.66</td>
<td>4.3</td>
<td>2.66</td>
</tr>
<tr>
<td></td>
<td>C6 5.57</td>
<td>6.2</td>
<td>4.15</td>
</tr>
</tbody>
</table>

From Fig. 3-9 and Table 3-7, one can see that \( R_{\text{ON}} \) depends on the anneal temperature and the recess step. For the shallow and the partial recess, \( R_{\text{ON}} \) increases when the temperature increases from 350 \( ^{\circ}\text{C} \) to 400 \( ^{\circ}\text{C} \), then decreases at 450 \( ^{\circ}\text{C} \) and increases again at 500 \( ^{\circ}\text{C} \), regardless of \( L_{\text{AC}} \) and FP length. As for the full recess, the same tendency is observed from 350 \( ^{\circ}\text{C} \) to 400 \( ^{\circ}\text{C} \) and 450 \( ^{\circ}\text{C} \). \( R_{\text{ON}} \) increases from 350 \( ^{\circ}\text{C} \) to 400 \( ^{\circ}\text{C} \), then decreases at 450 \( ^{\circ}\text{C} \). However, \( R_{\text{ON}} \) decreases from 450 \( ^{\circ}\text{C} \) to 500 \( ^{\circ}\text{C} \) when the FP length is 4 \( \mu\text{m} \) and increases in the case of 2 \( \mu\text{m} \) FP.

It is obvious that \( R_{\text{ON}} \) increases with \( L_{\text{AC}} \). \( R_{\text{ON}} \) varied between 1.56 m\(\Omega\).cm\(^2\) to 3.34 m\(\Omega\).cm\(^2\) for \( L_{\text{AC}} \) of 15 \( \mu\text{m} \), 2.66 m\(\Omega\).cm\(^2\) to 5.81 m\(\Omega\).cm\(^2\) for \( L_{\text{AC}} \) of 20 \( \mu\text{m} \) and 2.27 m\(\Omega\).cm\(^2\) to 10.3 m\(\Omega\).cm\(^2\) for \( L_{\text{AC}} \) of 25 \( \mu\text{m} \), regardless of the FP length. In the latter case (\( L_{\text{AC}} \) of 25 \( \mu\text{m} \)), the large variation of \( R_{\text{ON}} \) is caused by the diodes position on the 2x2 cm\(^2\) sample (discussed later).

We have shown that \( R_{\text{ON}} \) increases with \( L_{\text{AC}} \). Zhu et al. \(^{63}\) have reported on the increase in \( R_{\text{ON}} \) from 3.7 m\(\Omega\).cm\(^2\) to 5.12 m\(\Omega\).cm\(^2\) when the distance \( L_{\text{AC}} \) increases from 20 \( \mu\text{m} \) to 25 \( \mu\text{m} \), respectively, using Ni/Au full recessed anode. In our study, in similar process conditions to ref. \(^{63}\) (2 \( \mu\text{m} \) FP length and anode full recess), \( R_{\text{ON}} \) increased from 3.26 m\(\Omega\).cm\(^2\) to 4.89 m\(\Omega\).cm\(^2\).
when the distance \( L_{AC} \) increases from 20 µm to 25 µm, respectively, after annealing at 450 ºC. Consequently, our results are close or even slightly better to the state of the art.

- **Forward characteristic dispersion**

  It is important to mention that the forward I-V characteristics depends on the SBD position on the 2x2 cm\(^2\) sample. The dispersion was also recess-dependent, meaning that when the recess depth is deeper, the dispersion is highlighted. The variation was observed for the majority of the samples and affected mainly \( R_{ON} \). \( R_{ON} \) increases when the SBD placement is closer to the edge of the sample. Fig. 3-10 shows the worst-case J-V characteristics of the sample full recessed and annealed at 400 ºC. The anode-cathode distance is 15 µm and the FP length is 4 µm. Fig. 3-10 also shows one of the extreme dispersion in our study. When the distance between the SBD and the center of the sample increases, \( R_{ON} \) increases too. \( R_{ON} \) varied from 1.88 mΩ.cm\(^2\) to 4.72 mΩ.cm\(^2\) with a median value of 2.62 mΩ.cm\(^2\).

![Current density against forward voltage for full recessed sample annealed at 400 ºC.](image)

**Fig. 3-10.** Current density against forward voltage for full recessed sample annealed at 400 ºC. This dispersion is an extreme one from our study. \( R_{ON} \) is degraded when the diode is closer to the sample edge.

To summarize the forward bias measurements, the full recessed samples exhibit the highest barrier heights for the same anneal temperature. These samples also exhibit the lowest ideality factors, lower than 2, meaning that the thermionic emission dominates the current transport. The full recessed samples also show the lowest \( V_{ON} \) between 0.64 V and 0.73 V, which is comparable to the literature when using only a Ni anode. \( R_{ON} \) depends on the anneal temperature and the recess, however, with no clear tendency. On the other hand, \( R_{ON} \) increases with \( L_{AC} \). The lowest \( R_{ON} \) was obtained for the shallow recessed sample annealed at 450 ºC. \( R_{ON} \), in most of the cases, is comparable to the values reported in the literature.
3.3.2 Reverse bias

Other important parameters, such as the leakage current and the breakdown voltage, are extracted from the reverse bias measurements as presented in Fig. 3-11.

![Graph showing reverse bias characteristic](image)

**Fig. 3-11. Parameters extraction from the reverse logarithmic I-V characteristic.**

The leakage current represents the current losses in blocking mode. In this mode, the leakage current must be as low as possible, even at high voltage (-600 V), to reduce losses in the blocking mode. On the other hand, at the breakdown voltage, the leakage current increases rapidly to reach very high values. At this voltage, the device is overheated by the accelerated carrier circulation. The breakdown, also called avalanche process, occurs by impact ionization of the carriers. At high voltages, when the electric field reaches the critical electric field of the material, the carriers gain high energy by the external electric field and are accelerated. Consequently, the collision between the carriers and the ionized atoms creates more carriers. Once the breakdown is achieved, the phenomenon is non-reversible and the device is damaged.

3.3.2.1 Leakage current

Fig. 3-12 shows the median leakage current density (of all the SBDs) versus the reverse voltage up to 400 V for all the samples. The shallow (Fig. 3-12a), partial (Fig. 3-12b) and full recess (Fig. 3-12c) are represented by the full, dashed and dotted lines, respectively.
Fig. 3-12. The median leakage current density versus the reverse voltage up to 400 V for all the samples.
(a) The shallow, (b) partial and (c) full recess are represented by the full, dashed and dotted lines, respectively.

First, we can compare the effects of the recess at a given temperature from Fig. 3-12a, b and c. At 350 °C, the partial (Fig. 3-12b) and full (Fig. 3-12c) recesses result in the lowest current density of 4.5x10⁻¹ µA.mm⁻¹ at 400 V, 100 times lower than the current density obtained after the shallow recess (Fig. 3-12a). At 400 °C, the shallow and partial recesses result in a current density 100 times higher than the one obtained after the full recess (8.4x10⁻² µA.mm⁻¹ at 400 V). At 450 °C, the full recess also results in current density (8.9x10⁻² µA.mm⁻¹) approximately 100 times lower than the other recesses at 400 V. Finally, at 500 °C, the shallow recessed sample shows an immature breakdown (sample eliminated in our further discussions), while the full recessed one results in a current density (1.2 µA.mm⁻¹) 10 times lower than the partially recessed one at 400 V.

The next paragraph discusses the effect of the anneal temperature at a given recess. For the shallow recessed samples (Fig. 3-12a), with the exception of the sample annealed at 500 °C and its immature breakdown, the leakage current density is similar upon any anneal temperature. In Fig. 3-12b (partial recess), J_R increases with the anneal temperature up to 450 °C and decreases slightly upon annealing at 500 °C to reach 10 µA.mm⁻¹, considered as a high leakage current density at 400 V. The low J_R of 5x10⁻¹ µA.mm⁻¹, reached upon annealing at 350 °C can be
explained by the high barrier height of 0.77 eV. Nevertheless, the lowest leakage current at any anneal temperature is reached after the full recess (Fig. 3-12c) of the Schottky contact. At 400 V, $J_R$ decreases from $4.5 \times 10^{-1}$ µA.mm$^{-1}$ at 350 ºC to $8.4 \times 10^{-2}$ µA.mm$^{-1}$ at 400 ºC and increases slightly to $8.9 \times 10^{-2}$ µA.mm$^{-1}$ at 450 ºC, and reaches the highest value for the full recessed SBDs of 1.2 µA.mm$^{-1}$ at 500 ºC. Once again, the full recessed samples show the most interesting characteristics.

These conclusions are also presented in Fig. 3-13 which shows the leakage current density $J_R$ (expressed in A.mm$^{-1}$) at -100 V, -200 V, -300 V and -400 V extracted from the characteristics of C1 diodes (15 µm L$_{AC}$ and 4 µm FP length) for all the samples. $J_R$ is extracted from a group of 1 to 5 similar SBDs.

![Fig. 3-13. The leakage current density versus the recess and anneal temperature at different reverse voltages. The red, blue, orange and black dots correspond the leakage current density at -100 V, -200 V, -300 V and -400 V, respectively.](image)

We observe the same tendencies discussed in Fig. 3-12. From Fig. 3-13, we conclude that when the reverse bias increases, $J_R$ increases for all samples. The leakage current increases with the voltage up to 300 V by approximately one order of magnitude every 100 V. Above 300 V, $J_R$ reaches a stable value until the breakdown occurs.

The Schottky barrier height, independent from the anode-cathode distance and the FP length as reported previously, is an obstacle to the electron circulation in the reverse mode. Consequently, the leakage current depends mainly on the barrier height and varies slightly with the anode-
cathode distance and the FP length. Thus, Fig. 3-13 is representative of all the SBDs from the same sample (Table 4-3). $J_R$ varies slightly as function $L_{AC}$ and the FP length. The maximum variation from $5.4 \times 10^{-8}$ A.mm$^{-1}$ to $1.7 \times 10^{-7}$ A.mm$^{-1}$ was observed for the full recessed sample (Fig. 3-12c) annealed at 400 °C.

### 3.3.2.2 Breakdown voltage

Before discussing the breakdown voltage, a summary of the electrical parameters extracted or calculated from the J-V characteristics is necessary. The full recessed samples exhibited the highest barrier height at any given temperature. The highest barrier of 0.89 eV and 0.88 eV were obtained upon annealing at 400 °C and 350 °C, respectively. The same process conditions showed the lowest ideality factor of 1.49 and 1.55, respectively. They also exhibited the lowest $V_{ON}$ that varied between 0.64 V and 0.73 V. On the other hand, the partial recessed samples annealed at 350 °C and 450 °C exhibited the lowest $R_{ON}$. As for the leakage current density, the full recessed samples annealed at 350 °C, 400 °C and 450 °C presented the lowest $J_R$. The sample annealed at 500 °C showed a high $J_R$ of 1.2 µA.mm$^{-1}$ at 400 V. The lowest the leakage current is, the lower the losses are during the devices operations (energy economy). The partial recessed one, annealed at 350 °C, exhibited a low leakage $J_R$ of approximately 0.5 µA.mm$^{-1}$ at 400 V, making from it an interesting sample. This sample also showed a relatively high barrier height of 0.85 eV. $R_{ON}$ varied between 2.26 mΩ.cm$^2$ and 5.49 mΩ.cm$^2$. However, the main inconvenients of this sample are the high $V_{ON}$ between 1.09 V and 1.13 V and especially the high ideality factor of 2.54, meaning that the recombination is limited by both carrier types. Thus, this sample which will not be considered for further analysis.

Table 3-8 presents each sample with the corresponding electrical parameters. The positive sign means that the parameter value is a desired one while the negative sign means the opposite. The blank means that the parameter is equivalent to the majority of the samples.
Table 3-8. The Schottky recess applied and the corresponding anneal temperature as a function of the extracted electrical parameters.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Shallow (4 nm)</th>
<th>Partial (15 nm)</th>
<th>Full (30 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anneal temperature (°C)</td>
<td>350</td>
<td>400</td>
<td>450</td>
</tr>
<tr>
<td>φ_B</td>
<td>-</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>n</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>V_ON</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>R_ON</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Leakage at -400 V</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Desired parameter values</td>
<td>1+</td>
<td>2+</td>
<td>1+</td>
</tr>
</tbody>
</table>

*R_ON is high only for C5 and C6 SBDs. R_ON of other SBDs is comparable to the other samples.

From Table 3-8, we can conclude that the full recessed samples annealed at 350 °C, 400 °C and 450 °C present the maximum number of positive signs. Consequently, the breakdown voltage of these samples will be discussed in the next paragraph.

The maximum blocking voltage a device can handle is a very critical parameter for all high power devices. The high (theoretical) electric field of 330 V.µm⁻¹ makes from GaN an interesting material. This electric field is 10 times higher than the one of Si.

Firstly, the SBDs were measured in the reverse mode up to -600 V. Unfortunately, many breakdowns have occurred before 600 V. However, some SBDs handle this voltage without breakdown. Consequently, quantifying the breakdown voltage is still difficult. Table 3-9 presents the median breakdown (if occurred) of the SBDs from each sample and the number of the SBDs between brackets. The SBDs that have handled the 600 V are marked with “ >600 ” and the number of the SBDs is also marked between brackets.
Table 3-9. The median $V_{BR}$ (if occurred) of the SBDs from the full recessed samples, annealed at 350 °C, 400 °C and 450 °C. The “>600” refers to the SBDs that handled 600 V and the number of the SBDs between brackets. In both cases, the number between brackets corresponds to the SBDs number.

<table>
<thead>
<tr>
<th>Recess</th>
<th>Annealing temperature</th>
<th>Breakdown voltage (V) (number of SBDs)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>C1</td>
</tr>
<tr>
<td>Full (30 nm)</td>
<td>350 °C</td>
<td>490±30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(5)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;600</td>
</tr>
<tr>
<td></td>
<td>400 °C</td>
<td>553±39</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(6)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;600</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3)</td>
</tr>
<tr>
<td></td>
<td>450 °C</td>
<td>463±5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;600</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1)</td>
</tr>
</tbody>
</table>

Fig. 3-14 shows the average breakdown voltage, of every SBDs achieving the breakdown before 600 V, plotted versus the anneal temperature of the full recessed samples.

For SBDs with 4 µm FP length (C1, C2 and C3), $V_{BR}$ increases slightly with the distance $L_{AC}$, with the exception of C2 when annealed at 400 °C. In fact, three C2 SBDs from the sample annealed at 400 °C did not reach breakdown up to 600 V (Table 3-9), explaining the lower average $V_{BR}$ of these diodes in Fig. 3-14. Nevertheless, the effect of $L_{AC}$ on $V_{BR}$ for SBDs with 2 µm FP length (C4, C5 and C6) is not clear. For the samples annealed at 350 °C and 450 °C, $V_{BR}$ increases when $L_{AC}$ increases from 15 µm to 20 µm and then decreases for $L_{AC}$ of 25 µm. The sample annealed at 400 °C showed a similar $V_{BR}$ for $L_{AC}$ of 15 µm and 20 µm and a $V_{BR}$ increase for $L_{AC}$ of 25 µm.
Fig. 3-14. The average breakdown voltage, of every SBDs achieving the breakdown before 600 V, plotted against the anneal temperature of the full recessed samples.

Taking into account all our results, it is clear that the highest breakdown voltages were observed for the sample annealed at 400 °C. Fig. 3-15 shows the best reverse electrical results of this sample corresponding to SBDs with $L_{AC}$ of 25 µm. the full blue line corresponds to the 4 µm FP while the dotted line corresponds to the 2 µm one.

Fig. 3-15. $J_R$ as a function of the reverse bias for the full recessed sample annealed at 400 °C. The blue line corresponds to the best C3 SBD while the dotted red line corresponds to the best C6 SBD.

$V_{BR}$ depends on the FP length. For the 4 µm FP, a 760 V breakdown voltage was observed with 0.06 µA.mm$^{-1}$ leakage current density before the breakdown. $V_{BR}$ decreases when using a 2 µm FP length to reach 660 V and 0.16 µA.mm$^{-1}$ leakage current density before the breakdown. Depending on the passivation layer thickness, the optimal FP length may vary. In our case, the
optimal FP length is definitely higher than 2 µm. However, it might be lower or higher than 4 µm.

### 3.3.3 Comparison with the state of the art

A state of the art of SBDs electrical parameters extracted from the literature is provided in Table 3-10.
Table 3.10. State of the art on SBDs processed on the AlGaN/GaN heterostructure.

<table>
<thead>
<tr>
<th>Epitaxy</th>
<th>Schottky contact (nm)</th>
<th>LAC FP length</th>
<th>( V_{ON} ) (V)</th>
<th>( \phi_B ) (eV)</th>
<th>( n )</th>
<th>( J_R ) at -400 V</th>
<th>( V_{BR} ) (V)</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN 20%</td>
<td>Ni</td>
<td>12 µm</td>
<td>0.50</td>
<td>0.71</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>25 nm</td>
<td></td>
<td>2 µm</td>
<td>1.47</td>
<td>1.13</td>
<td></td>
<td>-</td>
<td>-</td>
<td>13 *</td>
</tr>
<tr>
<td>Si(111) 4''</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 mA.cm(^{-2}) for L(_{AC}) of 12 µm</td>
<td>1020</td>
<td></td>
</tr>
<tr>
<td>AlGaN 25%</td>
<td>Pt/Ti/Au 40 nm-recess</td>
<td>2-18 µm</td>
<td>0.43</td>
<td>0.43</td>
<td>1.72</td>
<td>1 μA.mm(^{-1}) for L(_{AC}) of 15 µm</td>
<td>&gt;1000 (J(_R) of 10 μA.mm(^{-1}) at 1000 V)</td>
<td>115 **</td>
</tr>
<tr>
<td>26 nm</td>
<td></td>
<td>1 µm</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>in-situ SiN</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ni</td>
<td>Non recessed</td>
<td>1.74</td>
<td>1.07</td>
<td>1.76</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AlGaN 25%</td>
<td>Pt/Ti/Au 35 nm</td>
<td>2-18 µm</td>
<td>0.5</td>
<td>0.62</td>
<td>1.40</td>
<td>-</td>
<td>-</td>
<td>84 **</td>
</tr>
<tr>
<td>25 nm</td>
<td>Recess</td>
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<tr>
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<td></td>
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</tr>
<tr>
<td>Ni</td>
<td>Non recessed</td>
<td>1.25</td>
<td>0.97</td>
<td>1.67</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
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<tr>
<td>AlGaN 26%</td>
<td>Ni(30)/Au(50)</td>
<td>10-15 µm</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10 μA.mm(^{-1})</td>
<td>~800</td>
<td>43 ***</td>
</tr>
<tr>
<td>18 nm</td>
<td></td>
<td>1 µm</td>
<td></td>
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<tr>
<td>Si(111)</td>
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<td></td>
</tr>
<tr>
<td>AlGaN 24%</td>
<td>Ni (300)</td>
<td>25 µm</td>
<td>0.7</td>
<td>0.89</td>
<td>1.49</td>
<td>8.4x10(^{-2}) μA.mm(^{-1})</td>
<td>760</td>
<td>Our study ****</td>
</tr>
<tr>
<td>26-29 nm</td>
<td>Recess</td>
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<td></td>
<td></td>
<td></td>
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</tbody>
</table>

*Ti/Al/Ti/Au ohmic contact annealed at 850 °C for 30 sec under N\(_2\)*

**Ti/Al/Mo/Au ohmic contact annealed at 830 °C*

***Ti (25 nm)/Al (105 nm) ohmic contact annealed at 830 °C for 1 min

****Ti (70 nm)/Al (180 nm) ohmic contact annealed at 800 °C for 3 min

Chang et al. have reported on a dual metal at the anode that resulted in a 0.74 eV barrier for an ideality factor between 1.38 and 1.82 and a \( V_{ON} \) of 0.57 V on 25 nm Al\(_{20\%}\)GaN. They have also reached a high \( V_{BR} \) of 1020 V and a high leakage current of 1 mA.cm\(^{-2}\) for a 12 µm anode-
cathode distance. Bahat et al. 84,115 have reported in two different studies a barrier height of 0.62 eV and 0.43 eV and an ideality factor of 1.40 and 1.72 using a Pt/Ti/Au 35 nm and 40 nm recessed Schottky contact, respectively, on 25 nm Al_{25}\%Ga_{75}\%N. They have also reported a $V_{BR}$ (>1000 V) for a leakage current of 10 $\mu$A.mm$^{-1}$). Akkaya et al. 43 have reported a 1 eV barrier height for a 1.34 ideality factor using Ni/Au contact on 18 nm Al_{26}\%Ga_{74}\%N. In our study, an Al_{24}\%Ga_{76}\%N barrier of 26 nm to 29 nm epitaxied on 8 in. Si (111) substrates is used to process Au-free SBDs. The AlGaN at the anode region is fully recessed and the 300 nm Ni layer is sputtered on the GaN channel. The sample annealed at 400 ºC featured the best electrical results. We report a Schottky barrier height of 0.89 eV, an ideality factor of 1.49. These results are similar to the one reported in the literature using a recessed anode region. Furthermore, $V_{ON}$ of 0.7 V is practically independent on $L_{AC}$. As for the leakage current density, we report one of the lowest median $J_R$ of 8.4x10^{-2} $\mu$A.mm$^{-1}$ at high reverse voltages. Concerning $V_{BR}$, many SBDs did not reach the breakdown up to 600 V, while, for others, a 760 V breakdown was reached. Comparing to the literature, $V_{BR}$ is still limited due to the design of our circular diodes. The FP also plays an important role. A double or triple field plate results in a higher breakdown. Zhu et al. 63 have reported on a double FP resulting in a 1.9 kV breakdown voltage of a SBD on the AlGaN/GaN heterostructure. Despite the importance of the breakdown voltage in power devices, minimizing the leakage current is crucial since low power consumption is of an important consideration. To our knowledge, such a very low leakage current density resulting from our study has never been reported before on SBD processed on the AlGaN/GaN heterostructure epitaxied on Si, without compromising the forward characteristic.

3.3.4 Design optimization

In this first phase, our design was a simple circular diode and, hence, needs to be optimized. Finger diodes for example give more accurate results using our heterostructures. The design also plays a key role in reducing the leakage current and $V_{ON}$. Many approaches have been suggested to reduce $J_R$ and $V_{ON}$. Among these approaches, a dual metal combination of high and low work functions 13,116, recessed Schottky 70, etc. were proposed. The first option is the gated ohmic anode structures that consist in a Schottky contact physically connected to an ohmic electrode without a parasitic region 73 as presented in Fig. 3-16a (Type I). The authors have fabricated recessed and conventional SBD for comparison (Fig. 3-16b, Type II and Fig. 3-16c, Type III).
Fig. 3-16. Cross-sectional schematics of AlGaN/GaN-on-Si rectifiers. (a) Rectifier with a gated ohmic anode (type I), (b) recessed SBD (type II), and (c) conventional SBD (type III). Both anode and cathode contact areas are 80×100 µm². Type I has a 3-µm-wide recessed region. Distance from the recessed edge to the Schottky overhang edge is 2 µm in types I and II.¹⁷³

For 18 µm L_AC, V_ON increased from 0.37 V to 0.57 V and 1.06 V, for SBD type I, II and III, respectively. The forward current density at 1.5 V decreased from 92.2 mA.mm⁻¹ to 71.3 mA.mm⁻¹ and 32.5 mA.mm⁻¹, for SBD type I, II and III, respectively. However, V_BR is practically identical to all SBD types.

Another interesting design is the edge terminations reported by Hu et al.⁵⁸ to optimize J_R and V_ON. Fig. 3-17 shows (a) external edge terminated-SBD (EET-SBD) and (b) gated edge terminated-SBD (GET-SBD). The anode recess on both structures was applied to leave only 5 nm of AlGaN under the anode. Fig. 3-17c shows a conventional SBD for comparison.
Fig. 3-17. Cross-sectional schematics of AlGaN/GaN-on-Si SBDs with edge terminations: (a) External Edge Terminated (EET)-SBD, (b) Gated Edge Terminated (GET)-SBD and (c) conventional SBD.

At the forward bias, GET-SBD showed the most interesting on-state characteristics with the lowest $V_{ON}$ of 1.15 V at 100 mA.mm$^{-1}$. On the other hand, EET-SBDs show two orders of magnitude reduction in the leakage current at -100 V as compared with the reference SBDs due to the additional AlGaN barrier recess at the edge terminations which reduces the 2DEG density. The GET-SBD featured the lowest leakage current. The latest presented a 1 µA.mm$^{-1}$ at -600 V and a breakdown voltage around -850 V for an $L_{AC}$ of 10 µm.

In Chapter 2, we have reported a dependence between the electrical results and the epitaxy (strain, $x_{Al}$, etc.). Consequently, even though that some of our electrical results were better than the one reported in the literature (in particular, the leakage current), it may be promising to process the SBDs in our conditions (metal layers, recess, etc.) while improving our design (i.e. using a GET structure).
3.4 Conclusions

In this chapter, we fabricated Schottky diodes on the heterostructure. Based on the results of Chapter 2, the ohmic contact metals, recess and annealing were fixed to be Ti (70 nm)/Al (180 nm) partially recessed and annealed at 800 °C for 3 min, resulting in a 2.8 Ω.mm and a sheet resistance of 480 Ω/sq. The total passivation (SiN-3) thickness is 250 nm deposited by PECVD. The Schottky contact consists in a 300 nm Ni layer sputtered by PVD. During the process, shallow, partial and full anode recesses were studied. The metal layer was annealed between 350 °C and 500 °C for each recess. Finally, the circular SBDs anode-cathode distance and the field plate length were varied to understand their effect on the electrical characterization of the SBDs from each sample.

The shallow recessed samples annealed at 350 °C, 450 °C and 500 °C exhibited low barrier heights. The partial recess exhibited scattered barrier height values, depending on the applied temperature. The highest barrier of 0.85 eV was obtained upon annealing at 350 °C. Full recessing the anode resulted in the highest barrier heights at any given temperature. The full recessed structures showed the lowest ideality factor especially after annealing at 400 °C (1.49). This sample presented also the highest barrier height of 0.89 eV.

\( V_{ON} \) decreased when the anneal temperature increased, for the same recess depth. \( V_{ON} \) is significantly reduced after annealing at 500 °C, regardless of the recess depth, meaning that the high temperature annealing helps diffusing the metal into the AlGaN layer (in the case of shallow and partial recess) resulting in a low \( V_{ON} \). The lowest \( V_{ON} \) is achieved after full recess, at a given temperature and varied between 0.64 V and 0.73 V. This can be attributed to closeness between the anode and the 2DEG. However, in this case, \( V_{ON} \) variation depending on \( L_{AC} \) is practically negligible.

For shallow and partial recesses, \( R_{ON} \) increases when the temperature increases from 350 °C to 400 °C, then decreases at 450 °C and increases again at 500 °C, regardless of the \( L_{AC} \) and the FP length. As for full recess, \( R_{ON} \) increases from 350 °C to 400 °C, then decreases at 450 °C. However, \( R_{ON} \) decreased from 450 °C to 500 °C when the FP length is 4 µm and increases in the case of 2 µm FP. Moreover, \( R_{ON} \) varied from 1.56 mΩ.cm² to 3.34 mΩ.cm² for \( L_{AC} \) of 15 µm, 2.66 mΩ.cm² to 5.81 mΩ.cm² for \( L_{AC} \) of 20 µm and from 2.27 mΩ.cm² to 10.3 mΩ.cm² for \( L_{AC} \) of 25 µm.
At 350 °C, partial and full recesses resulted in the lowest current density at 400 V. At 400 °C, shallow and partial recesses resulted in a current density 100 times higher than the one obtained after full recess. At 450 °C, full recess also resulted in $J_R$ much lower than other recesses at 400 V. Finally, at 500 °C, shallow recessed sample showed an immature breakdown, while the full recessed one resulted in a current density 10 times lower than partial recessed one at 400 V. The lowest $J_R$ at any anneal temperature is reached after full recessing the anode. At 400 V, $J_R$ decreased from $4.5 \times 10^{-1}$ µA.mm$^{-1}$ at 350 °C to $8.4 \times 10^{-2}$ µA.mm$^{-1}$ and $8.9 \times 10^{-2}$ µA.mm$^{-1}$ at 400 °C and 450 °C, respectively, and increased to reach the highest value of 1.2 µA.mm$^{-1}$ at 500 °C.

The sample annealed at 400 °C featured the best electrical results after full recessing the anode. A Schottky barrier height of 0.89 eV and an ideality factor of 1.49 are obtained. Furthermore, $V_{ON}$ of 0.7 V is practically independent of $L_{AC}$. Furthermore, we report one of the lowest $J_R$ ($8.4 \times 10^{-2}$ µA.mm$^{-1}$) at high reverse bias, comparing to the state of the art. However, many SBDs reached the breakdown before 600 V, while for the best case, a 760 V breakdown was achieved, certainly related to our simple design and simplified process.

Optimizing the design will improve $V_{BR}$. For instance, a double or triple field plates results in a higher breakdown. Junction barrier Schottky (JBS)-like diodes (by p-type ion implantation) can also improve the breakdown voltage. It is worth mentioning that, to our knowledge, such very low leakage current density resulting from our study has never been reported before on SBD processed on the AlGaN/GaN heterostructure epitaxied on Si, without compromising the forward characteristic.
Chapter 4. Ion implantation and dopant activation
The process of a Schottky diode on the heterostructure has been presented in the previous chapter. In specific cases, localized doping is required to create n⁺ rich layers or p-type guard rings \(^2,117\) (see also Fig. 1-17). However, for power devices, the control of doping is a crucial issue. In particular, to achieve a high breakdown voltage and low specific ON-resistance devices on wide band gap materials, localized doped zone by ion implantation remains a Graal.

For GaN, the dopants most frequently used for n and p-type doping are Si and Mg, respectively. Up to now, researchers have largely reported high donor concentration in \textit{in-situ} doped or implanted Si in GaN \(^118\text{–}121\) while p-type doping using Mg in GaN is still an issue, in particular when using ion implantation. Ion implantation induces defects in GaN crystalline structure, thus, Mg activation requires firstly a recrystallization of GaN lattice, while Mg atoms settle in substitutional sites (Ga sites).

Although reaching an \textit{in-situ} Mg-doping in GaN \(^122\text{–}124\), after two decades of research, can be relatively easy, achieving an acceptor activation of implanted Mg in GaN is still extremely challenging. Unintentionally doped GaN always evidences a high electron concentration that requires a high dose of Mg to reach a p-type material. However, high dose implantation induces lattice disorder \(^125\), thus compensating or trapping the carriers and consequently resulting in low effective doping. The lattice recovery from implantation-induced damages can lead to efficient acceptor activation. GaN is very sensible at high temperature. Above 800 °C, nitrogen starts to out-diffuse from the surface leaving behind hexagonal pits unsuitable for devices fabrication. Thereby, protecting the GaN surface with a cap-layer is crucial prior to any high temperature thermal treatments \(^32\text{–}34\).

The first section of this chapter is dedicated to ion implantation issues namely the channeling of the dopants and the implantation-induced damages in GaN crystalline structure.

Afterwards, AlN and SiO\(_x\) cap-layers protecting the GaN surface during thermal treatments will be presented. The structural characterization and the surface morphology of the AlN layer after deposition will be discussed.

The third section explains the high temperature thermal treatments used and their effect on the GaN surface after cap-layers chemical etch.

Finally, low and high temperature annealings effect on GaN:Mg protected by AlN/SiO\(_x\) double cap-layer are presented in this section. Detailed characterizations using XRD, AFM and low temperature photoluminescence (LT PL) are discussed. The influence of laser irradiation at
different energies and number of pulses on the GaN surface morphology and dopant activation are presented.
4.1 Ion implantation issues in GaN

Doping is a key step in the process of any microelectronics components. A good control of the doping level is crucial to process reproducible and reliable devices. As discussed in Chapter 1, doping in GaN can be achieved in-situ during the epitaxy, where the entire layer is doped, or ex-situ by ion implantation. However, to achieve localized doped zones, ion implantation is one of the solutions. Although reaching an in-situ Mg-doping in GaN can be relatively easy, achieving an acceptor activation of implanted Mg in GaN is still extremely challenging. Unintentionally doped GaN always evidences a high electron concentration that requires a high dose of Mg to reach a p-type material. Furthermore, high energies are required to achieve the desired doping profile. Consequently, ion implantation induces defects in GaN crystalline structure. Furthermore, channeling mechanism upon ion implantation is prevailing. In fact, dopants are found deeper in the layer than expected. The researchers have found the solution for the channeling mechanism in Si. Tilting the ion beam and using a pre-implantation amorphous layer are widely studied.

4.1.1 Channeling of Mg dopants

Multiple implantations are required to obtain a box-like profile for Mg implantation. A depth of 300-400 nm of p-type zone with 1x10²⁰ cm⁻³ Mg plateau is required to form guard rings under the Schottky contacts (Fig. 1-15). In GREMAN, simulations were done using 3 different implantation energies in order to reach the box-like Mg profile as shown in Fig. 4-1. However, Fig. 4-1 also compares the simulation profile with the experimental results obtain by secondary ion mass spectroscopy (SIMS). Clearly, the simulation results are different than the measured ones. While the simulation shows a quasi-abrupt junction at approximately 400 nm, an implantation tail reaching 1 µm of depth is visible with a high Mg concentration. It is worth to mention that the implantation is done with 7 ° tilt and without a pre-implantation sacrificial layer. Different solutions are proposed in the literature to reduce this implantation tail such as 10 ° tilt or even silicon oxide pre-implantation layer.
Fig. 4-1. Triple implantation simulation and experimental (SIMS) comparison. The implantations were processed at 40 keV, 80 keV and 160 keV with respectively, $2 \times 10^{14}$, $4 \times 10^{14}$ and $1.5 \times 10^{15}$ atoms.cm$^{-2}$.

### 4.1.2 Ion implantation induced damages

Khalfaoui$^{117}$ has studied Mg ion implantation and activation in GaN and has reported the degradation of the GaN layer quality after triple energy implantation. Fig. 4-2 shows a STEM of GaN sample after implantation. A 200 nm thick damaged layer is clearly visible in the cross section image.

Fig. 4-2. STEM image of Mg implanted GaN sample. A 200 nm thick damaged zone is visible in the cross section view$^{117}$.

High temperature thermal treatments are necessary to activate implanted dopants and to reduce the implantation-induced defect density. However, due to the sensibility of GaN at high temperatures, unprotected GaN surface is totally damaged as can be observed in Fig. 4-3 after
annealing 2 min at 1150 °C. Nitrogen desorption leaves behind a Ga-rich surface with a high roughness.

Fig. 4-3. Optical microscope image showing the degraded surface of GaN after annealing at 1150 °C for 2 min without cap-layer.

To overcome these obstacles, the protection of GaN during thermal treatments with a cap-layer is essential. To avoid confusing the damages caused by the implantation or by the high temperature annealing, we firstly studied cap-layers on non-implanted GaN samples. Consequently, any damage caused to the surface is strictly related to the cap-layer and the applied annealing. Once the optimal cap-layer found, we applied different annealings on GaN:Mg samples.

4.2 Cap-layers study on non-implanted samples

The ideal cap-layer must have a low lattice mismatch with GaN to limit the stress, a good mechanical and chemical stability at high temperature. It must also reduce the nitrogen gradient between the GaN surface and the atmosphere to limit nitrogen desorption from GaN film. It must also not contaminate GaN layer (i.e. introducing dopants such as Si and oxygen or passivating atoms such as hydrogen) and must be selectively etched without damaging the GaN surface.

Several approaches for this cap-layer have been proposed with partial success: gallium oxide, gallium oxinitride, boron nitride (BN), SiOₓ, or AlN. Therefore, there are large studies on AlN reported in the literature. Considering the lattice mismatch between GaN and AlN (2.4%), cracks may appear through AlN layer providing path for N₂ to out-diffuse from GaN thus leaving behind a damaged surface. In order to avoid these cracks, a compromise should be found among AlN growth parameters. Hager et al. have studied MOCVD and sputtered AlN on GaN and have compared surface states before and after annealing at high...
temperatures (>1100 °C). They have reported that dual AlN layers annealed over 1250 °C evidenced cracks and that hexagonal pits appeared on GaN surface after AlN layers etch. Greenlee et al. have studied different MOCVD AlN and sputtered AlN (low and high temperature) encapsulants for high temperature GaN annealing. They have reported that MOCVD cap performed unsatisfactory results. They also reported that the MOCVD + high temperature sputtered cap resulted in a 99.4% decrease in thermal etch pits compared to just MOCVD AlN cap. However, pits were still observed on the surface of annealed GaN by optical microscopy.

4.2.1 AlN reactive magnetron sputtering

In our study, we deposited AlN layers by reactive magnetron sputtering. This technique allows the deposition at a relatively low temperature (700 °C), lower than the GaN critical one (820 °C). Furthermore, the resulting layers are less strained than MOCVD or MBE ones. Consequently, thicker crack-free AlN layers can be deposited on GaN.

The GaN films used in this study were grown by MOCVD on 6 in. Si (111) substrates. The samples consisted of 5 μm thick n type GaN doped at 7×10¹⁵ cm⁻³ on a 2 μm thick n⁺ type GaN (1×10¹⁸ cm⁻³). Due to the lattice mismatch and thermal expansion difference between the GaN epilayer and the substrate, a buffer layer was introduced to reduce dislocation density. Wafers were cut into samples (1.4×1.4 cm²) and cleaned using “clean 1” (refer to Chapter 1).

Our design of experiments consisted in depositing various AlN layers by Physical Vapor Deposition (PVD) using Direct Current (DC) reactive magnetron sputtering using a 99.9995% pure Al metal target 80 mm distant from samples. High vacuum was reached in the chamber before pre-sputtering the Al target for 5 min using Ar was performed followed by the introduction of N₂ to obtain the desired gas composition, reaching a total working pressure of 5 mTorr. According to the significant differences of sputtering conditions observed in the literature, we investigated a large range of the deposition parameters of our equipment aiming to obtain crack-free layers. Therefore, AlN was sputtered under powers ranging from 100 W to 900 W, at temperatures ranging from 300 to 700 °C under N₂ – Ar atmospheres. A first group of samples was deposited according to the conditions given in Table 4-1. the sputtering duration was fixed to 10 min.
Table 4-1. First group of experimental cases for AlN growth on GaN during 10 min at 5 mTorr.

<table>
<thead>
<tr>
<th>Sample name</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>A4</th>
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<th>A6</th>
<th>A7</th>
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<tbody>
<tr>
<td>Temperature (°C)</td>
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<td>550</td>
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<tr>
<td>Power (W)</td>
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<td>500</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>500</td>
<td>900</td>
</tr>
<tr>
<td>N₂/Ar gas flow ratio</td>
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<td>2/1</td>
<td>2/1</td>
<td>2/1</td>
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<td>Cracked</td>
<td>Crack-free</td>
<td>Cracked</td>
<td>Cracked</td>
</tr>
</tbody>
</table>

After the deposition, cap-layers were then analyzed to understand the exact composition, the surface morphology and the crystalline structures.

EDS has been also used to detect Al peak on the surface before and after AlN etching.

Thicknesses were measured by SEM after focused ion beam (FIB) sample cross sectioning. Depending on the parameters values, thicknesses have been observed in the range of [30–400] nm. It is important to mention that the only crack-free AlN layer after sputtering (and before any thermal treatment) is the one deposited at the highest temperature and the lowest power with a 0.5 N₂/Ar ratio (sample A6).

Fig. 4-4 shows two SEM images of AlN layers deposited on GaN with different conditions. In Fig. 4-4a, the 130 nm AlN layer grown at 700 °C, 500 W is cracked and also partially lifted off while Fig. 4-4b shows the only crack-free 30 nm thick AlN layer previously described (sample A6). This AlN layer is also the thinnest AlN layer in this set of experiments.

Fig. 4-4. SEM images of (a) 130 nm cracked AlN with unsticking AlN layer in the insert, and (b) 30 nm crack-free AlN.
Samples were then separated in different groups in order to observe the effect of each parameter on the layer (thickness, quality). Regardless of the temperature and the plasma power, AlN thickness is always lower when N₂/Ar gas flow ratio is in favor of nitrogen. Moreira et al. 131 have studied the effect of nitrogen flow and plasma power on AlN layers deposited on Si (100). They have reported that, when increasing N₂ flow in N₂/Ar gas mixture, AlN thickness was reduced. In addition, they have also reported that the AlN thickness increases with the plasma power, regardless of the N₂ flow and/or the growth temperature. In our experiments, a 30 nm thick AlN layer is obtained at the highest temperature and the lowest power and nitrogen flow. At 500 W, AlN thickness increases to reach 180 nm, while at 900 W, AlN thickness reaches 370 nm. This behavior occurs due to the higher concentration of Al extracted from the target with higher plasma power.

The temperature effect on AlN thickness is not as strong as the one observed for the two other parameters. AlN thickness slightly decreases from 170 nm to 160 nm and 130 nm when the temperature increases. Kuang et al. 135 have studied the effect of temperature (300 °C, 500 °C and 700 °C) on AlN grown by Radio Frequency PVD. They have reported a slight reduction of the thickness when temperature increases. Furthermore, they have observed that the lowest roughness of as-deposited AlN is found when the growth temperature rises.

The highest AlN layer thickness has been measured for sample grown with the lowest temperature and N₂ flow and the highest power while the lowest AlN layer thickness, as mentioned before, has been grown with the lowest plasma power and N₂ flow conditions but with the highest growth temperature.

However, 7 samples out of 8 exhibited cracked AlN layer after sputtering. Based on these observations, the second set of samples has been designed targeting a thickness around 20 nm. This is in agreement with the fact that the strain increases generally with thickness when depositing a layer of AlN on GaN due to the lattice mismatch (2.4%) 132,136. Considering, as a first approximation, a linear deposition rate, new growth durations were determined to obtain 20 nm of AlN for all the previous cases. Table 4-2 shows the deposition conditions of the second set of samples with the resulting thicknesses extracted by SEM/FIB observations.
Table 4-2. The second group of experimental cases at 5 mTorr targeting 20 nm thick AlN layers growth on GaN, with the corresponding thickness, layer state and RMS roughness.

<table>
<thead>
<tr>
<th>Sample name</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
<th>B4</th>
<th>B5</th>
<th>B6</th>
<th>B7</th>
<th>B8</th>
</tr>
</thead>
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<tr>
<td>Temperature (°C)</td>
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<td>300</td>
<td>300</td>
<td>550</td>
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<td>700</td>
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<tr>
<td>Power (W)</td>
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<td>900</td>
<td>500</td>
<td>500</td>
<td>500</td>
<td>100</td>
<td>500</td>
<td>900</td>
</tr>
<tr>
<td>N₂/Ar gas flow ratio</td>
<td>1/2</td>
<td>2/1</td>
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<td>2/1</td>
<td>2/1</td>
<td>1/2</td>
<td>1/2</td>
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<tr>
<td>Deposition time (sec)</td>
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<td>39</td>
<td>71</td>
<td>75</td>
<td>92</td>
<td>400</td>
<td>76</td>
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<tr>
<td>Thickness</td>
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<td>21 nm</td>
<td>21 nm</td>
<td>20 nm</td>
<td>27 nm</td>
<td>19 nm</td>
<td>34 nm</td>
<td>40 nm</td>
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<tr>
<td>Layer state</td>
<td>Randomly cracked</td>
<td>Cracked</td>
<td>Cracked</td>
<td>Cracked</td>
<td>Cracked</td>
<td>Crack-free</td>
<td>Cracked</td>
<td>Rough</td>
</tr>
<tr>
<td>RMS roughness (nm)</td>
<td>0.75</td>
<td>0.65</td>
<td>0.46</td>
<td>0.75</td>
<td>1.08</td>
<td>0.37</td>
<td>0.87</td>
<td>7.78</td>
</tr>
</tbody>
</table>

Once again the same influence of growth parameters on AlN thickness have been observed in this second set of experiments. Taking into consideration differences between the sputtering durations: an increase in the plasma power leads to a thicker AlN layer while a thinner one is observed when increasing nitrogen flow or deposition temperature.

AFM was performed to determine surface state and roughness. RMS roughness (10x10 μm²) are reported in Table 4-2 while surface AFM images are presented in Fig. 4-5 with the corresponding sample name. Samples B1-B7 showed low roughness AlN layers. However, sample B8 exhibited a roughness of 7.78 nm. Moreover, it is obvious that the roughness increases with the temperature. These results are compatible with the one reported by Moreira et al. 131 indicating a rougher surface when the plasma power increases.

Nevertheless, AFM images showed cracks appearing at the surface even when AlN thickness reaches 20 nm. Only 2 deposition conditions resulted in crack-free AlN layers (sample B1 and B6). However, sample B1 deposited at 900 W, 300 °C and a gas ratio of ½ is unstable. These deposition conditions were not kept due to the difficulties to reproduce a systematic stable deposition process. Sample B1 can randomly lead to cracked or crack-free AlN layer after the deposition. Nevertheless, it is important to mention that, once again, only one deposition condition led to a systematically smooth and crack-free layer (sample B6, deposited in the same conditions of sample A6 with shorter growth duration).
XRD has been used to identify eventual crystalline phases of AlN on all samples. Fig. 4-6 shows the XRD spectra of (a) a GaN reference sample, (b) an AlN on GaN deposited at the lowest temperature and N₂ flow and the highest power (sample B1), (c) an AlN on GaN deposited at the lowest power and N₂ flow and the highest temperature (smooth and crack-free, sample B6). Taking into consideration the presence of the Si (111) substrate, buffer layers and the GaN (0002) from the epitaxial layer, no additional peak appears when comparing (a) reference sample to (b) sample B1 spectra. Nevertheless, a new peak at about 37.5 ° appears on the spectra of sample B6. Cheng et al.¹³⁷ have done XRD measurements on AlN deposited under various N₂ concentrations on Si (100). They have reported the presence of different AlN peaks depending on N₂ concentration evidencing the deposition of crystalline AlN by reactive sputtering means. They also have found that under low nitrogen concentration (25%), the AlN showed (100) preferred orientation. Increasing the nitrogen concentration up to 75%, resulted in layers with a mixture of (100), (101) and (001) orientations. In our study, the new peak corresponds to the formation of a (001)-oriented AlN layer. The peak appearance at 37.5 ° can be explained by the presence of Oxygen in this layer. Nevertheless, the peak appearance (crystalline layer), combined with the thickness of the layer, could explain why this layer is crack-free.
Fig. 4-6. X-ray diffraction spectra: 0-20 scans of (a) GaN reference without AlN, (b) GaN sample after AlN growth at the lowest temperature and gas flow and the highest power (sample B1) and (c) GaN sample after AlN growth at the lowest power and gas flow and the highest temperature (sample B6), respectively. Spectra are vertically shifted for clarity reasons.

To investigate further the crystalline quality of this layer, transmission electron microscopy (TEM) has been carried out on sample B6 with 19 nm of AlN thickness. TEM image presented in Fig. 4-7 shows a crystalline AlN layer deposited on GaN. However, it is very difficult to identify the interface AlN/GaN even with high resolution images (Fig. 4-7b).

Fig. 4-7. HR-TEM images (a) of GaN/AlN interface and (b) AlN layer.

In fact, due to the high deposition temperature of the AlN layer (700 °C), Al atoms diffuse in GaN first layers forming an AlGaN alloy. X-ray photoelectron spectroscopy (XPS) is carried on sample B6 to analyze the surface composition. Fig. 4-8 shows the presence of Al (green line), Ga (violet line) and nitrogen (red line) at the interface AlN/GaN. Instead of having a sharp
interface, the Al composition gradually decreases while the Ga one increases, resulting in an AlGaN layer between the AlN and the GaN layers.

Fig. 4-8. Surface composition analysis of sample B6 by XPS.117.

Time-of-flight secondary ion mass spectroscopy (Tof-SIMS) also confirmed this conclusion as presented in Fig. 4-9. The Al atoms penetrate in the GaN layer and form an AlGaN layer after depositing the AlN layer at 700 °C. This AlGaN layer can be a bottleneck during the cap-layer etching step after high temperature annealing.

Fig. 4-9. Tof-SIMS analysis of the GaN sample after depositing an AlN layer at 700 °C.

4.2.2 Silicon oxide cap-layers

It is known that oxide capping is not an efficient way to protect the surface.34 In addition to the appearance of pits, oxygen and Si diffusion in GaN are suspected to modify the electrical state at the surface.34 As a consequence, a double cap-layer, including AlN previously defined (B6) with a 200 nm SiOx capping on top, has been experimented. SiOx on AlN allows to increase the thickness of the cap-layer with the benefit of a thin crystalline crack-free AlN layer. AlN is also
expected to protect GaN surface and to prevent from oxygen and Si diffusion into GaN coming from SiO$_x$ with benefit of a double cap-layer.

### 4.3 Thermal treatment and cap-layer etching

Upon ion implantation, the GaN layer is damaged as shown previously. Consequently, thermal treatments are required for the recovery from the implantation-induced damages and to activate dopants (such as Mg). In this section, we will present the results obtained after high temperature thermal treatments on GaN samples protected with cap-layers. The cap-layers etching upon annealing will also be presented in order to investigate the GaN surface integrity and to verify their efficiency.

#### 4.3.1 Annealings

Two different types of annealing were investigated: Single-cycle RTA (S-RTA) and Multi-cycle RTA (M-RTA)\textsuperscript{138}. The S-RTA consists in annealing at 1150 °C for 3 min in N$_2$ with a 1.4 °C.s$^{-1}$ ramp slope to reach the final temperature while the M-RTA consists in a 1.4 °C.s$^{-1}$ ramp slope to 700 °C followed by a rapid increase of the temperature between 700 °C and 1180 °C (80 °C.s$^{-1}$) and a cooling to 700 °C, repeated 15 times. Using this process, GaN is exposed for a short time to high temperatures above the thermodynamic stability. However, Feigelson et al.\textsuperscript{138} have already mentioned that, without any cap-layer, even for such a short time, GaN surface is markedly degraded.

- **Single cap-layer**

Firstly, S-RTA was performed on GaN samples capped with AlN from Table 4-1. SEM images of the surface after annealing S-RTA using AlN deposited in different conditions are presented in Fig. 4-10.

![Fig. 4-10. SEM images of the surface after annealing S-RTA using AlN deposited in conditions of (a) A7 and (b) A8, respectively.](image-url)
Samples with initially cracked AlN layers are entirely damaged and evidenced larger cracks after annealing regardless of the layer thickness. The AlN layer is also partially ripped from the surface, depending on the sample, leaving behind an unprotected GaN areas during thermal treatments. SEM observations showed that GaN surface was partially or totally damaged after S-RTA. Each time, AlN cap-layer was cracked and GaN surface was damaged after annealing.

GaN samples capped with cracked AlN from Table 4-2 exhibited the same surface as in Fig. 4-10 upon S-RTA and will not be presented here. Sample B8, with initially a rough AlN surface, exhibited a high hexagonal pits density (not shown here). These conclusions show clearly that rough and cracked AlN layers are not efficient cap-layers for GaN surface protection.

Concerning initially crack-free sample A6, both types of annealing (S-RTA and M-RTA) were performed. Contrary to results reported by Feigelson et al. 138, hexagonal pits appeared on the surface after thermal treatments in both cases, as shown in Fig. 4-11. SEM images were also used to calculate pit density that has been estimated to 9.89x10^5 and 1.48x10^6 pits.cm^{-2} for S-RTA and M-RTA, respectively, with larger pits diameter in the case of M-RTA evidencing that M-RTA damages GaN surface more than S-RTA.

![SEM images of sample A6 after (a) S-RTA (hexagonal pit in the inset) and (b) M-RTA.](image)

Both annealings were also applied on sample B6. AFM measurements on as-deposited and annealed samples are presented in Fig. 4-12. One can observe that the low roughness (around 0.37 nm) of the as-deposited sample increases up to 1.22 nm after S-RTA. Hexagonal pits appear after both thermal treatments with densities of 1.79x10^6 and 1.41x10^6 pits.cm^{-2}, respectively, for S-RTA and M-RTA.

Nevertheless, pit density, in our study between 9.89x10^5 and 1.79x10^6 pits.cm^{-2}, can be considered as low compared to 2x10^6 and 1.6x10^7 pits.cm^{-2} for GaN/sapphire and GaN/Si...
substrates, respectively, after a 2 min RTA at 1150 °C with a 200 nm thick TEOS (Tetra Ethyl OrthoSilicate) cap-layer, deposited by PECVD, reported by Bazin et al. 121.

![Figure 4-12](image)

Fig. 4-12. 10x10 µm² AFM images of sample B6: (a) as deposited AlN, (b) after S-RTA and (c) after M-RTA.

- **Double cap-layer**

As seen previously, hexagonal pits appear after any thermal treatment and the surface roughness increases. However, Schottky contacts are strongly sensitive to surface state. Thus, high quality Schottky contacts cannot be processed on such a surface. Consequently, a double cap-layer was deposited and both types of thermal treatments were applied. This cap-layer consists in a 20 nm AlN layer in conditions of B6 followed by a 200 nm PECVD SiOₓ. SiOₓ was removed in HF (10%) solution after thermal treatments. Fig. 4-13 shows 10x10 µm² AFM images of annealed samples (B6) after SiOₓ etching compared with as deposited AlN, in the inset EDS showing Al peak appearance. Roughness increases from 0.37 to 0.47 and to 0.61 nm, after S-RTA and M-RTA, respectively. Samples annealed with double cap-layer show lower roughness than samples annealed with a single AlN cap-layer (Fig. 4-12). Furthermore, single AlN cap-layer samples exhibited hexagonal pits through the AlN layer. Annealing with a double cap-layer showed no pit appearance. To confirm this conclusion, the annealed AlN layer has to be efficiently etched without deteriorating the GaN surface.
Fig. 4-13. 10x10 µm² AFM images of (a) sample B6 as-deposited (EDS after deposition in the inset) (b) double cap-layer after S-RTA and SiOₓ etching and (c) double cap-layer after M-RTA and SiOₓ etching.

4.3.2 Double cap-layer etching

Based on literature 139–142, wet etching was subsequently processed on AlN capped samples in a KOH solution (KOH:H₂O = 1:4) from room temperature up to 80 ºC and in a H₃PO₄ solution at 120 ºC. Mileham et al. 142 have reported AlN etching grown on Al₂O₃ in an AZ400K photoresist developer solution, based on a KOH buffered solution. They have found that the etch rate is strongly dependent on the crystalline quality of the AlN. In our study, not only AlN layer was etched but also GaN surface was attacked and damaged as shown in Fig. 4-14. KOH solution is not an appropriate solution due to the low selectivity between AlN and GaN.

Fig. 4-14. SEM images of GaN surface after etching in KOH at room temperature.

Ababneh et al. 140 have reported the etching of sputtered AlN under different conditions in an 85% H₃PO₄ solution at 80 ºC. Hsu et al. 94 have studied the etch of non-polar GaN in a mixture of H₃PO₄/H₂SO₄ at 160 ºC for 20 min. They have reported that the etch pits of a-plane GaN are more like nanopipes, which start at the N-facet {000-1} and terminate at the Ga-facet {0001}. Thus, pure H₃PO₄ solution etches N-polarity GaN films very quickly, resulting in the complete removal of surface morphology. Furthermore, Zhang et al. 143 have studied HVPE GaN etch in H₃PO₄. They have reported that no change occurred after 5 min in H₃PO₄ at 210 ºC. They have
also reported GaN etch in H$_3$PO$_4$ at 230 °C. After 3 min, hexagonal pyramid shape appears. After 6 min, hexagonal prism shape appears on surface and after 9 min, huge etch pits are brought to light. The etch temperature in our study, 120 °C, is too low to etch GaN. Furthermore, etching tests were done on GaN in the same etchant of AlN using SiO$_x$ as a mask. AFM image in Fig. 4-15a shows GaN surface after 10 min in H$_3$PO$_4$ at 120 °C. No etching step has been observed between protected and unprotected GaN surfaces. Moreover, atomic steps are clearly visible and RMS roughness is very similar to the GaN reference one (after cleaning).

Fig. 4-15. 10x10 µm$^2$ AFM images of (a) GaN surface after 10 min in H$_3$PO$_4$ solution at 120 °C and (b) sample B6 S-RTA annealed after SiO$_x$ and AlN etching (EDS after AlN etch in the inset).

AlN etch was proceeded in H$_3$PO$_4$ solution during 10 min at 120 °C. Al peak, detected before the etching step by EDS disappeared after etching. Furthermore, XRD peak at 37.5 °, corresponding to the AlN deposited layer, also disappeared after the etch evidencing the efficiency of H$_3$PO$_4$ solution for AlN removal. Moreover, AFM image (Fig. 4-15b) shows a smooth GaN surface where the atomic steps are visible and a relatively low roughness of 0.91 nm compared to the roughness of GaN reference sample (0.34 nm). Finally, no hexagonal pit is observed on the surface. SEM images confirm this result on a large observation surface of GaN (not presented here). These results evidence the efficiency of this double cap-layer for GaN protection. This process has been reproduced several times with the same efficiency. To our knowledge, an effective double cap-layer to protect the GaN surface at 1150 °C has never been reported before.

4.4 Mg ion implantation in GaN for p-type doping

Until now, our study was developed on GaN samples before Mg ion implantation. We showed the efficiency of an AlN (20 nm)/SiO$_x$ (200 nm) double cap-layer in the protection of GaN at
high temperature annealing (S-RTA and M-RTA). However, ion implantation induces damages in GaN crystalline structure, thus Mg activation requires firstly a recrystallization of the GaN lattice at low temperatures (< 820 °C) before activating Mg atoms at high temperatures. Another approach consisted in laser irradiating the samples at low energies. Both techniques will be discussed later-on.

In this section, a 900 nm c-plane oriented thick-GaN layer was grown by MOCVD on 8 in. Si (111) substrate provided by supplier C. Multiple Mg-implantations were performed with different energies and a total dose of 3x10^{15} cm^{-2} at 300 K in order to form a box-like profile (see Fig. 4-1).

### 4.4.1 Low temperature furnace annealing

Low temperature annealing (LTA) consists in a 10 °C.min^{-1} temperature ramp up to reach 800 °C followed by a 12 or 24 hours plateau. The samples can be annealed at this temperature for long duration without any surface protection. The implanted GaN surface morphology was monitored by AFM before and after annealing and cap-layer removal. Fig. 4-16 shows GaN surface after ion implantation and after LTA without and with cap-layers, respectively. The RMS roughness is very low and remains the same.

![AFM images of implanted GaN surface](image)

**Fig. 4-16.** 10x10 µm² AFM images of implanted GaN surface (a) before and (b) after 12 h LTA, (c) 24 h LTA without cap-layer and (d) 12 h LTA with cap-layers.

Samples were subject to a θ-2θ scan before and after LTA. The XRD spectra show the existence of a damage induced by Mg-implantation, as revealed by the apparition of the satellite peak of the epitaxied Wurtzite GaN (0002) shown in Fig. 4-17, at a smaller angle (34.4 °), meaning that the lattice of GaN has slightly expanded according to c-axis. Furthermore, GaN (0002) peak shifts to a slightly smaller angle (34.57 °) upon implantation (reference not presented here). After applying the LTA for 12 h, the satellite peak is still observed with a shift to higher angle,
indicating a limited recovery from implantation. The LTA for 24 h recovers further the GaN lattice. Even though the GaN satellite peak shifts to higher angle after 12 h LTA, GaN (0002) FWHM slightly increases (of 8 arcsecs). This can be explained by the fact that the partial recovered GaN layers diffract at a very close angle of the epitaxied GaN (0002) resulting in a slightly broader FWHM.

![XRD spectra](image)

Fig. 4-17. XRD spectra of (a) as-implanted, (b) LTA samples for 12h and (c) for 24 h, respectively. Spectra are vertically shifted for clarity reasons.

RSM was performed on the GaN (-1-124) reflection in order to understand the effect of implantation and LTA on the a and c-axis of the GaN layer. Fig. 4-18a shows the RSM of as-implanted sample where the satellite peak appears under the GaN (-1-124) one. Both peaks are aligned according to q_x axis confirming the previous conclusion and meaning that the implantation damages occur essentially according to c-axis. The GaN satellite peak disappears after both LTA (12 and 24 h). However, when comparing both annealings (Fig. 4-18b and c), the GaN (-1-124) takes an asymmetric quasi-elliptic shape only upon 24 h annealing, meaning that annealing for 24 h at 800 ºC, results in a better GaN lattice recovery after ion implantation.
The optical characterizations of the annealed samples are then performed using LT PL spectroscopy. The samples were excited with a 325 nm/3.8 eV laser of He-Cd with an excitation power of 1 mW. The PL spectrum was recorded at 4.5 K from red (2 eV, 620 nm) to near UV (3.5 eV, 354 nm). We expect no Mg activation after such annealings. In fact, activating Mg dopants certainly requires higher temperatures (> 1100 ºC). Consequently, PL of LTA samples (see Fig. 4-22 for PL spectrum of sample LTA for 12 h), did not exhibit any significant signal in the range [2-3.5 eV] similarly to the as-implanted GaN (not shown here). Damages caused by the implantation introduce defects into the band gap. These defects result in a non-radiative recombination, by interacting with phonons or in a radiative recombination by emitting photons in a different range. Consequently, LTA single-handedly, as expected, does not lead to any Mg activation.
### 4.4.2 Multi-temperature annealing

To activate Mg dopants in GaN, high temperatures annealings are required. S-RTA and M-RTA (described in 3.3.1) are applied on GaN:Mg. Some samples also combine both LTA and RTA. Table 4-3 shows the different thermal treatments applied on GaN:Mg samples. All samples were capped with AlN (20 nm)/SiO$_x$ (200 nm) double cap-layer for the GaN surface protection.

<table>
<thead>
<tr>
<th>Nº of sample</th>
<th>Annealing</th>
<th>Annealing conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I1</td>
<td>S-RTA</td>
<td>1150 °C for 3 min</td>
</tr>
<tr>
<td>I2</td>
<td>M-RTA</td>
<td>15 cycles of temperature rapid increase between 700 °C and 1180 °C (stabilization for 5 s)</td>
</tr>
<tr>
<td>I3</td>
<td>24 h LTA + S-RTA</td>
<td>24 h LTA followed by S-RTA</td>
</tr>
<tr>
<td>I4</td>
<td>12 h LTA + S-RTA</td>
<td>12 h LTA followed by S-RTA</td>
</tr>
<tr>
<td>I5</td>
<td>12 h LTA + M-RTA</td>
<td>12 h LTA followed by M-RTA</td>
</tr>
</tbody>
</table>

In order to avoid redundancy, the surface morphology after high temperature thermal treatments are presented in section 4.3.1 after the cap-layer etch. Only AFM images of sample I3 (highest thermal budget) are presented in Fig. 4-19. On the 10x10 µm$^2$ images, the atomic steps are visible and the roughness slightly increases. However, on the 2x2 µm$^2$ images, the roughness increases to 0.49 nm and the atomic steps are hardly visible.

![Fig. 4-19. 10x10 and 2x2 µm$^2$ AFM images of (a) as-implanted GaN surface and (b) sample I3 after cap-layer etch.](image)

After higher temperature annealing (sample I1), the satellite peak disappears as revealed by XRD spectra in Fig. 4-20. Moreover, GaN (0002) peak is reinstated to the initial position (before implantation). Both peak shifting evidence a higher GaN lattice recovery. The satellite peak disappearance and GaN peak shift have also been observed on XRD spectra of I2, I3, I4.
and I5 (not shown here), confirming that high temperature annealing partially recovers GaN damaged-lattice.

**Fig. 4-20.** XRD spectra of (a) as-implanted, (b) 12 h LTA, (c) 24 h LTA and (d) S-RTA samples, after cap-layers removal. Spectra are vertically shifted for clarity reasons and dotted line helps elucidate GaN peak shift.

RSM was performed on all samples to understand further the effect of the thermal treatments on the lattice recovery and the dopants activation. After high temperature annealing, the satellite peak disappears and the GaN (-1-124) reflection adapts a symmetric elliptic form as shown in Fig. 4-21.
We previously studied the effect of the annealing on the GaN surface and crystalline structure. We concluded on the efficiency of high temperature annealings for GaN lattice recovery from implantation induced damages. Nevertheless, understanding the mechanism giving the rise to optical signature of GaN:Mg could be capital for enhancement of Mg activation. In the literature, GaN:Mg PL results are still debated. Depending on growth technique, doping level and applied annealing conditions, complex behaviors have been observed by PL. Two Mg related acceptors in GaN with similar binding energy have been reported: unstable acceptor related to Mg-H complexes and regular stable one upon annealing (Mg substitutional at Ga site). Ironically, as mentioned by Lany et al., lattice relaxed, noneffective-mass state are responsible for the p-type conductivity rather than the shallow effective-masslike state. Consequently, two different luminescence bands dominate the GaN:Mg PL spectrum: a broad blue luminescence (BL) band peaking between 2.7-3.0 eV or an ultra-violet luminescence (UVL) band with a maximum at 3.2-3.3 eV. Donor-acceptor pair (DAP) transition is responsible for BL and UVL bands. DAP transition implicates a shallow MgGa acceptor and a shallow donor or a deep donor for ULV and BL bands, respectively.
Fig. 4-22. Excitation intensity dependent PL spectra of Mg-implanted GaN after 12 h LTA and samples I1, I2, I4 and I5 from Table 4-3.

Fig. 4-22 shows the excitation intensity dependent PL spectra (discussed later on) for the sample LTA for 12h and I1, I2, I4 and I5 (Table 4-3). We have studied two different intensity dependences of the PL: 1 and 100% of the total intensity with 0.5 and 0.05 sec acquisition time, respectively. The intensity is related to the thickness $x$ by the following equation:

$$I = I_0 \cdot e^{-\alpha x}$$

Eq. 3.1

where $I_0$ and $\alpha$ are the initial intensity and the GaN absorption coefficient, respectively. Therefore, at 325 nm of laser wave length, the excitation intensity decreases by a factor of ten every 220 nm considering GaN absorption coefficient at about $10^{5} \text{cm}^{-1}$ \[150,151\].

Regardless of the optical filter used, RTA samples exhibit a yellow/green luminescence (mentioned as YL) band [2-2.5 eV] stretching out to an identical maximum in all cases as shown in Fig. 4-22. YL does not show a direct dependence related to the annealing procedure. The presence of YL is generally associated to carbon or hydrogen contamination/doping, gallium vacancies $V_{Ga}$ and/or recombination between O$_N$ and $V_{Ga}$ \[125,152-155\].

Moreover, depending on the annealing applied and the intensity of the PL measurement, acceptor related bound excitons (ABX) dominating the near band gap are observed at 3.446 eV and 3.452 eV (Fig. 4-23a-c), labeled as ABX2 and ABX1, respectively. According to the literature \[122,145,147\], ABX2 is suggested to be related to neutral ABX or Mg related deep ground state while ABX1 is attributed to a transitional Mg BX or unknown impurity. At 0.01 mW of intensity, ABX2 is slightly visible for I1 and I2 with a very low intensity while ABX1 transition occurs for I4. I5 exhibits an unidentified peak at 3.437 eV (Fig. 4-23c). When increasing the intensity to 1 mW, ABX2 dominates the near band gap for all samples, regardless of the
annealing applied (Fig. 4-23a). Additionally, one phonon replica 1LO-ABX is observed at 96 meV from ABX2 only for S-RTA samples (I1 and I4).

Monemar et al. 147 have reported on correlation between an ABX and DAP at 3.27 eV. They have concluded that both are most likely related to the same acceptor. PL peak position between 3.1 and 3.27 eV related to DAP transitions is attributed to Mg doping 149. In our study, at low intensity, there is no clear evidence of DAP for I2 and I5 due to interference fringes. The UVL band ranging from [3.1-3.3] eV is broad with intensity relatively equal to YL band. S-RTA samples I1 and I4 exhibit DAP peaks at 3.234 and 3.242 eV, respectively, as shown in Fig. 4-23d. At higher intensity (Fig. 4-23b), with the exception of I5 spectrum, 3.245 eV DAP transition overlaps the UVL band and dominates the PL spectra. Furthermore, as a result of coupling LTA and S-RTA, I4 evidences the highest DAP intensity.

It is worth to mention that all spectra have small oscillations from 3.2 eV to weaker energies. These oscillations are due to the PL measurement angle. Thus, it is difficult to identify, in some cases, DAP recombinations and the associated phonon replica due to these interference fringes.

Fig. 4-23. Excitation intensity dependent PL normalized spectra of Mg-implanted GaN (a) near band gap, (b) UVL band for high excitation intensity of 1 mW, (c) near band gap and (d) UVL band for low excitation intensity of 0.01 mW.
Oikawa et al. \cite{156} have studied Mg ion implantation in GaN epitaxied on free-standing GaN substrate. They have reported the presence of a 3.29 eV Mg related DAP emission and an ABX at 3.47 eV in their PL spectrum. They have also reported a P-N junction and a blue light-emission of implanted and annealed samples.

Leroux et al. \cite{145} have studied LT PL on weakly p-type (room temperature free hole concentration below $1 \times 10^{17}$ cm$^{-3}$) MBE-grown GaN. They have reported a near band edge excitonic peak assigned to ABX and a broad band near 3.27 eV was observed on their spectra. In our case, I4 exhibits a PL spectrum similar to the weakly p-type MBE-grown GaN reported in ref. \cite{145}.

Comparing I1 to I2 and I4 to I5, the presence of a clear DAP peak in the cases of I1 and I4 leaves a doubtless conclusion that the S-RTA is more efficient than the M-RTA. On the other hand, ruling out M-RTA samples, a higher DAP peak is observed for I4. Thus, even if LTA shows no luminescence, S-RTA assisted by LTA shows beneficial effects on Mg activation.

Definitely, a PL study on sample I3 was going to be interesting. Unfortunately, this sample was processed after the complete PL investigations on previous samples (sample I1, I2, I4 and I5). It is widely known that PL measurements are very sensitive and have to be carried out under similar conditions, thus it will be unfair to compare this new sample with the previous ones.

### 4.4.3 Laser irradiation

Another approach for dopant activation is the laser irradiation. This technique consists in a KrF (248 nm) laser source with a pulse duration of 25 ns. Samples in this section were laser irradiated by Dr. Joachim Bergmann and Dr. Gudrun Andrä from IPHT Jena. First, sacrificial samples were irradiated to evaluate the effect of the energy on the GaN surface with and without cap-layer. Two samples were then irradiated with AlN (20 nm)/SiO$_x$ (200 nm) double cap-layer and the other two were kept without protection. Consequently, a summary of all samples is presented in Table 4-4.
Table 4-4. Samples number with corresponding laser energy and number of pulses.

<table>
<thead>
<tr>
<th>No of sample</th>
<th>Laser energy and number of pulses</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>Without cap-layer irradiated 1 pulse at 300 mJ.cm$^{-2}$</td>
</tr>
<tr>
<td>L2</td>
<td>Without cap-layer irradiated 10 pulses at 250 mJ.cm$^{-2}$</td>
</tr>
<tr>
<td>L3</td>
<td>With cap-layer irradiated 1 pulse at 380 mJ.cm$^{-2}$</td>
</tr>
<tr>
<td>L4</td>
<td>With cap-layer irradiated 10 pulses at 380 mJ.cm$^{-2}$</td>
</tr>
</tbody>
</table>

Prior to the cap-layer deposition and the irradiation, the samples were subjected to “clean 1”. The GaN surface morphology was monitored by AFM before and after laser irradiation and Oxide removal (in the case of capped samples).

- Samples without cap-layers (L1 and L2):

According to the RMS roughness extracted from Fig. 4-24, we notice that no significant variation was observed before and after laser irradiation and chemical cleaning. The atomic steps are still visible. Furthermore, no hexagonal pit appears on the surface.

![AFM images](image)

Fig. 4-24. 10x10 µm$^2$ AFM images of GaN surface (a) after cleaning, (b) after 1 pulse irradiation at 300 mJ.cm$^{-2}$ and (c) after 10 pulses irradiation at 250 mJ.cm$^{-2}$.

XRD in plane scans was also performed on Mg-implanted samples before and after laser irradiation. Fig. 4-25 shows a 0-20 scan of GaN reference (after implantation) and samples L2 and L1, respectively. The satellite peak related to the implantation induced damages appears on the reference sample and is not influenced by the laser irradiation. The satellite peak remains visible regardless of the energy and the number of pulses. The FWHM of GaN (0002) reference and samples after laser irradiation (indicated in Fig. 4-25) does not reveal any significant modification before and after irradiation. Consequently, irradiating the samples in these conditions does not lead to any lattice recovery and dopant activation.
Fig. 4-25. XRD spectra of (a) GaN reference after implantation, (b) sample L2 and (c) sample L1, respectively. Spectra are vertically shifted for clarity reasons.

- Samples with cap-layers:

AFM images (Fig. 4-26) of irradiated samples (after oxide removal) showed no clear affection of the laser irradiation on the surface. The roughness insignificantly increases and the atomic steps are still visible. We shall note that in this case also no hexagonal pit appears on surface.

Fig. 4-26. 10x10 µm² AFM images of GaN surface (a) after cleaning, AlN surface (b) after 1 pulse at 380 mJ.cm⁻² and (c) after 10 pulses at 380 mJ.cm⁻², respectively.

Fig. 4-27 shows a 0-20 scan of GaN reference (after implantation) and samples L3 and L4 after irradiation. Once again, the satellite peak is still visible after laser irradiation as shown in the XRD spectra. Furthermore, the FWHM of GaN (0002) (indicated in Fig. 4-27 for all samples) shows no significant variation. However, depending on the number of pulses, the satellite peak shifts towards GaN (0002) peak. Although no significant recovery of implantation-induced
damage in GaN epi-layer is exhibited, the satellite peak shifting (of approximately 0.03 °) towards GaN (0002) peak can be interesting to carry further experiments.

Fig. 4-27. On the left, XRD spectra of (a) GaN reference after implantation, (b) sample L3 and (c) sample L4, respectively. On the right, XRD with a higher magnification at the interesting range. Spectra are vertically shifted for clarity reasons.

Based on these results, samples were irradiated 100, 500, 1000 pulses at the same energy and 1000 pulses at 500 mJ.cm⁻².

Fig. 4-28. XRD spectra of GaN reference after implantation, after irradiating at 380 mJ.cm⁻² 1 pulse, 10 pulses, 1000 pulses, 500 pulses, 1000 pulses and 1000 pulses at 500 mJ.cm⁻², from bottom to top.

Unfortunately, the GaN satellite peak is still observed without any further shift towards GaN (0002) peak. Consequently, no significant recovery of the lattice is achieved in such a case. Further investigations are required to fully understand the role of laser irradiation in GaN technologies.
4.5 Conclusions

To summarize, this chapter was dedicated to Mg ion implantation and dopant activation in GaN. In specific cases, Schottky diode process requires localized doping to create p-type guard rings. Furthermore, to activate implanted dopants, high temperature annealing is required. However, GaN surface is very sensitive at high temperatures. Consequently, the protection of the surface during thermal treatment with a cap-layer is mandatory.

AlN layers deposited by reactive sputtering were presented. An optimal crack-free layer was deposited at 700 °C, 100 W under N₂/Ar gas flow ratio of ½. However, we found that the AlN layer solely is inefficient and the GaN surface was degraded after thermal treatments. Thus, depositing a PECVD SiOₓ layer on top of the AlN one resulted in good surface protection upon annealing at 1150 °C. Conventional annealing at low temperature and RTA were firstly performed on GaN:Mg samples. The chemical etch of the cap-layer was studied. The SiOₓ layer was etched in an HF (10%) solution and the AlN layer was etched in an H₃PO₄ solution at 120 °C. The sample were characterized by AFM, XRD in the direct and the reciprocal and LT-PL.

Based on XRD spectra, we found a satellite peak of the GaN (0002) peak at smaller angle. This satellite peak is related to the implantation induced damages. It appears also on the RSM, showing the degradation of the GaN layer only along the c-axis. However, this peak shifts to higher angle after LTA (800 °C), showing a limited GaN lattice recovery. It disappears after high temperature annealings, meaning a partial recovery of the GaN lattice. Furthermore, GaN (0002) peak shift to the initial position before implantation. AFM images show a smooth and pit-free surface upon annealings and cap-layer etch. The atomic steps are visible and the roughness is close to the GaN reference.

The sample I4 annealed for 12 h at 800 C and S-RTA showed the most interesting PL results. ABX2 and ABX1 at 3.446 and 3.452 eV, respectively, dominated the near band gap. DAP peak was visible at 3.242 eV. According to the literature, ABX and DAP are related to the same acceptor, in our case, Mg acceptor. DAP transition involves an MgGa shallow acceptor and a shallow donor. It is important to mention that the LTA, solely, did not result in any luminescence in the range of [2-3.5] eV similarly to the as-implanted GaN. However, it is found that coupling LTA and S-RTA evidenced the highest DAP intensity and an improvement in the optical signature of Mg related acceptors by PL. Thus, optically activated Mg can be achieved.
by combining LTA and S-RTA. This result is of upraised significance for efficient power devices.

Laser irradiation was also performed on GaN:Mg samples. However, laser irradiation did not show promising results. Even though that GaN surface was not damaged after irradiation, the satellite peak slightly shifts (0.03 °) to higher angle after 10 pulses at 380 mJ.cm⁻². Furthermore, irradiating the samples 100, 500, 1000 pulses at the same energy and 1000 pulses at 500 mJ.cm⁻² did not exhibit any further recovery. The satellite peak is still observed and does not shift further towards GaN (0002) peak. Such laser irradiations are insufficient for an efficient Mg activation.
General conclusions

Until now Si is the main material used in power conversion applications. These applications require low losses (consequently, are energy saving), miniaturization and especially low cost. Indeed, Si-based devices are reaching their limits in this field. Wide band gap materials such as SiC and GaN started replacing Si. Nevertheless, despite the excellent properties and the devices performances already commercialized, SiC substrates are still too expensive. Thus, GaN has attracted researchers attention during the last decades. Initially, based on the wide direct gap, GaN is one of the most used material for blue and white LEDs. Consequently, the progress achieved on this material makes from GaN a very interesting candidate for power electronics and converters. In addition to the high electron saturation velocity, GaN high breakdown electric field makes from this semiconductor the future of power devices, especially when epitaxed on low cost substrates such as Si. Nowadays, the GaN epitaxy quality on large Si wafers is good enough to allow Schottky diodes development.

The objective of this work was to develop Schottky diodes on the AlGaN/GaN heterostructure epitaxied on 8” Si substrates. A high density and mobility 2-dimensional electron gas (2DEG) accumulates at the heterointerface, making from the heterostructure an interesting solution for power devices. From the passivation layers and the recess to the metal contacts and the ion implantation, we have conducted the study on each technological step to process power diodes.

We have deposited SiNₓ passivations by PECVD. We have found both Si-rich or N-rich layers with a refractive index higher or lower to the one of stoichiometric Si₃N₄ (2.01). We have also found that the layers can be in compressive or tensile stress depending on the deposition conditions. The most interesting SiNₓ layer is nitrogen-rich one with a very low tensile stress of 19 MPa. FTIR was done on the samples before and after annealing at 800 °C for 3 min. This annealing is used to form the ohmic contact, representing the highest thermal budget and will be discussed later on. We have also found, by FTIR, a decrease of N-H and Si-H stretching modes upon the annealing. Furthermore, Si-N asymmetric mode increases upon annealing, meaning that Si-N bonding increases. This SiNₓ layer was efficiently etched by RIE. AFM imaging have showed an invariant surface state and roughness of GaN/AlGaN before and after RIE of SiNₓ.
For the ohmic contact, we have focused on Au-free contacts (compatible with CMOS technology) such as Ti and Al. We have investigated the influence of the surface treatment, the annealing temperature and duration, the metal thickness and the AlGaN/GaN recess. In our study, we had different epitaxies from different suppliers. We have concluded that the electrical results under the same process conditions were epitaxy-dependent. We have found a recess-free and Au-free Ti (70 nm)/Al (180 nm) contacts with a very low contact resistance ($R_c$) of $1 \Omega \cdot$mm after annealing at a multi-temperature (500 °C for 3 min and 800 °C for 30 sec). However, we have found a contact resistance of $2.8 \Omega \cdot$mm on different heterostructure (partially recessed – 14 nm from the surface) using the same ohmic contacts annealed at 800 °C for 3 min. The specific contact resistivity and the sheet resistance were about $1.7 \times 10^{-4} \Omega \cdot$cm$^2$ and $480 \Omega$/sq, respectively.

Schottky to Schottky structures using 300 nm of Ni were fabricated and annealed at different temperatures and ambiances with different SiNx layers. These structures allow to study the Schottky contact while the other technological steps are still not developed. However, these structures give information only on the leakage current in blocking mode. On the recess-free heterostructure, the contacts annealed at 350 °C in $N_2$ have exhibited the lowest current densities of $1 \times 10^{-5}$ A.cm$^2$. EDS has showed a nitrogen-free Ni layer upon annealing at 350 °C while a N-rich layer was obtained after 550 °C annealing. On the other hand, the shallow recess exhibited the lowest leakage current density, using the SiNx passivation in slightly tensile strain (19 MPa).

Then, these technological steps were combined during the process to form circular diodes on the AlGaN/GaN heterostructure. The ohmic contact and the passivation were fixed while the Schottky contact depth (recess) and annealing temperature were varied. The sample annealed at 400 °C with 30 nm of etching depth showed the most interesting results. A Schottky barrier height of 0.89 eV, an ideality factor of 1.49 were observed. These diodes also exhibited a very low leakage current density (up to $-400$ V) of $8.45 \times 10^{-8}$ A.mm$^{-1}$. The breakdown voltage varied between 480 V and 760 V.

We believe that our results are very promising in the power conversion field. The very low leakage current combined with a high barrier height present a solution for the high losses of the current power devices in the blocking mode without compromising the forward bias. Nevertheless, considering the excellent theoretical properties of GaN, the components can still
be optimized. The design and the devices reliability are the perspectives subject to further investigations.

Honeycomb or interdigitated design can improve the components performance in reverse mode. A further study of the ohmic contact may result from a better contact resistance, and therefore a better forward characteristic. We intend to study the effect of varying Ti/Al ratio on the contact resistance as well as the surface treatment after etching the AlGaN layer. Furthermore, the study of different layers of passivation (deposition technique, thickness, etc.) may lead to trap reduction at the semiconductor/passivation interface and, consequently, an improvement in the electrical results. We also intend to deposit the first passivation layer by LPCVD at high temperature while reducing its thickness, as well as, trying other types of passivation, such as, hafnium oxide (HfO₂) or Titanium oxide (TiO₂).

One of the milestones of the Schottky diodes process on GaN is the p-type localized ion implantation. This p-type doping is used to improve the edge termination of the Schottky diodes and consequently to improve the electrical characteristics such as the breakdown voltage. The most used dopant for p-type GaN is Mg. To achieve a p-type material, high doses of Mg are required. However, high dose implantation induces lattice disorder. The lattice recovery from implantation-induced damages can lead to efficient acceptor activation. On the other hand, GaN is very sensible at high temperature. Above 800 °C, nitrogen starts to out-diffuse from the surface leaving behind hexagonal pits. These pits are unsuitable for devices fabrication. Thereby, protecting the GaN surface with a cap-layer is crucial prior to any high temperature thermal treatments. We have demonstrated reactive sputtering of an AlN layer on GaN at 700 °C with 100 W of plasma power. This AlN layer, combined with a SiOₓ one, deposited by PECVD, have showed a highly efficient double cap-layer after annealing the samples at 1150 °C for 3 min. AFM images of the GaN surface after the annealing have showed a smooth surface with a very low roughness, similar to the one before annealing. We have also showed the efficiency of a double temperature annealing (800 °C for 12 h and 1150 °C for 3 min) to partially recover the GaN lattice from the implantation induced damages and to activate the implanted Mg. XRD in the direct and reciprocal space have showed that the GaN (0002) satellite peak appearing after ion implantation (damages in the lattice), disappears after annealing. Furthermore, PL has revealed the presence of a donor-acceptor peak (DAP) at 3.242 eV. DAP involves an MgGa shallow acceptor and a shallow donor. In this section, we showed the importance of combining the low temperature annealing and the high temperature one.
Appendix A. Carrier transport mechanisms of metal-semiconductor

Depositing a metal on a semiconductor forms a potential barrier at the interface. When metal and semiconductor are considered separately, the energy difference between vacuum and Fermi levels in the metal is called metal work function \( q\Phi_M \) while electron affinity \( q\chi_S \) represents the difference between the vacuum level and the bottom of the conduction band (Ec) in n-type semiconductor (Fig. A-1a). When the metal and the n-type semiconductor are in contact and if \( q\Phi_M \) exceeds \( q\chi_S \), electrons from the semiconductor flow towards the metal, leaving behind a depletion region in the semiconductor. At the equilibrium, the Fermi levels are aligned and the semiconductor bands bend as shown in Fig. A-1b.

![Energy band diagrams for a metal and an n-type semiconductor](image)

Fig. A-1. Energy band diagrams for a metal and an n-type semiconductor (a) before any contact and (b) after contact at the equilibrium.

This band bending represents the potential barrier. Thus, the barrier height \( q\Phi_B \) depends on \( q\Phi_M \) and \( q\chi_S \) and is ruled by the following equation:

\[
q\Phi_B = q\Phi_M - q\chi_S \quad \text{Eq.A.1}
\]

An electric field appears in the depletion region \( W \) and reaches the maximum at the interface metal/semiconductor. In the case of n-type semiconductor, the depletion region depends on the doping level \( N_D \) of the semiconductor. Consequently, charge transport across the semiconductor is doping level-dependent. Three types of emissions take place: for low \( N_D \) \((< 1 \times 10^{17} \text{ cm}^{-3})\), for
intermediate $N_D$ ($1 \times 10^{17}$ to $1 \times 10^{19}$ cm$^{-3}$) and for high $N_D$ ($> 1 \times 10^{19}$ cm$^{-3}$). These emissions are illustrated in Fig. A-2.

For lightly doped semiconductor, the current flows as a result of the thermionic emission (TE) as shown in Fig. A-2a. The electrons are thermally excited over the barrier. Fig. A-2b represents semiconductor with an intermediate doping ($1 \times 10^{17}$ to $1 \times 10^{19}$ cm$^{-3}$) where the thermionic field emission (TFE) dominates the transport. At this range of doping, the barrier is sufficiently narrow to allow electron tunneling between the metal and the semiconductor. For highly doped semiconductor, the barrier becomes sufficiently narrow at the bottom of the conduction band that the electrons can tunnel directly. This emission is known as field emission (FE) and is shown in Fig. A-2c.

The characteristic energy $E_{00}$ is dependent on the doping level and expressed in Eq. A.2:

$$E_{00} = \frac{q h}{4 \pi} \sqrt{\frac{N_D}{\varepsilon \varepsilon_0 m^*}}$$

Eq. A.2

where $q$ is the electron charge, $h$ plank constant, $\varepsilon_0$ is the vacuum permittivity, $\varepsilon$ and $m^*$ are the permittivity and the electron effective mass of the semiconductor, respectively.

The temperature has also a major role on the transport mechanism. Thermionic emission dominates at high temperature ($kT \gg E_{00}$). At lower temperature ($kT \approx E_{00}$), thermionic field emission dominates the transport while at low temperature ($kT \ll E_{00}$), electron tunneling takes place and field emission becomes predominant.
Appendix B. Electrical characterization of ohmic contacts

Specific contact resistance and contact resistance

To characterize the ohmic contact, one should study the current circulation when applying a voltage (or vice versa). A good ohmic contact leads to a linear I-V curve with a low resistance value. However, the resistance is not sufficient to conclude on the good ohmic behavior. Another useful parameter to be extracted is the specific contact resistivity ($\rho_C$ in $\Omega \cdot \text{cm}^2$) also referred to as contact resistivity or specific contact resistance. $\rho_C$ is independent of the contact geometry. When using AlGaN/GaN heterostructure to process lateral devices (such as HEMTs), another useful parameter called contact resistance $R_C$ in $\Omega \cdot \text{mm}$ is calculated as function of $\rho_C$.

Generally, $\rho_C$ can be defined as expressed in Eq. B.1:

$$\rho_C = \left(\frac{\partial V}{\partial J}\right)_{V=0}$$  \hspace{1cm} \text{Eq. B.1}

where $V$ and $J$ are the bias applied and the current density, respectively.

$\rho_C$ can be simplified depending on the doping level (of n-GaN). For low doping, the current density is dominated by thermionic emission and $J$ is expressed by:

$$J = A^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right)$$  \hspace{1cm} \text{Eq. B.2}

where $A^*$ is the Richardson constant, Consequently, Eq. B.1 is simplified and shown in Table B-1 as function of the doping level and the emission mechanism.

<table>
<thead>
<tr>
<th>Emission mechanism</th>
<th>Doping level ($N_D$) in cm$^{-3}$</th>
<th>Specific contact resistivity $\rho_C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermionic emission</td>
<td>$&lt; 1 \times 10^{17}$</td>
<td>$\frac{k}{qA^*T} \exp\left(\frac{q\Phi_B}{kT}\right)$</td>
</tr>
<tr>
<td>Thermionic field emission</td>
<td>$1 \times 10^{17}$ to $1 \times 10^{19}$</td>
<td>$\sim \exp\left(\frac{q\Phi_B}{E_{00} \coth\left(\frac{E_{00}}{kT}\right)}\right)$</td>
</tr>
<tr>
<td>Field emission</td>
<td>$&gt; 1 \times 10^{19}$</td>
<td>$\sim \exp\left(\frac{\Phi_B}{\sqrt{N_D}}\right)$</td>
</tr>
</tbody>
</table>
Linear TLM

In 1964, Shockley \(^\text{157}\) introduced a technique to extract \(\rho_c\) by using transfer length method (TLM). This characterization technique helps finding not only \(\rho_c\) but also sheet resistance (Rsh) of the semiconductor underneath. Linear TLM (L-TLM) consisted in a series of rectangular metallic contacts distanced “d” from each other as shown in Fig. B-3. “d” increases between each 2 contacts and varies from few \(\mu\text{m}\) to few hundreds of \(\mu\text{m}\).

![Fig. B-3. Linear contact resistance structure where the grey regions represent the metal and the blue one represent the semiconductor (or passivation, if any). L and l are the length and the width, respectively, of the rectangular contacts distant “d” from each other.](image)

Using the four probes technique, when applying a bias between two contacts, the current enters from the first contact passes in the semiconductor and leaves from the second metal block. All metal blocks have the same dimensions, thus, resulting in the same resistance. Consequently, the total measured resistance is two times \(R_C\) and the resistance between the contacts (R\(S\)) (Eq. B.3):

\[
R_T = 2R_C + R_S
\]  
Eq. B.3

In our case, the contact is horizontal. The current flows tangentially to the contact and is distributed in an ununiformed way on the contact area. A high voltage appears near the contact edge and drops exponentially with the distance. This distance is known as transfer length \(L_T\) and can be expressed as follows:

\[
L_T = \sqrt{\frac{\rho_c}{R_{\text{sh}}}}
\]  
Eq. B.4

To estimate the transfer length, the sheet resistance and, consequently, the specific contact resistivity, one need to measure the resistance function of the contacts distance. This results in the following graph (Fig. B-4). More details on the equations are explained elsewhere \(^3,112\).
However, L-TLM has some inconvenient. For instance, the distance “δ” presented in Fig. B-3 can be non-negligible resulting in error when measuring $\rho_C$ and $R_{sh}$. Furthermore, the isolation of metallic contacts is necessary and leads to an extra step (etching or ion implantation).

**Circular TLM**

These issues can be avoided with Circular-TLM (C-TLM), consisting of circular metallic contacts of a diameter D and distance d from the outer metallic region as shown in Fig. B-5. The distance d varies from few microns to tens of microns. $\rho_C$ is more precise when measured using C-TLM.

![Fig. B-5. Circular contact resistance structure where the grey regions represent the metal and the blue ones represent the semiconductor (or passivation, if any). D is the diameter of the circular contacts distant “d” from outer metallic region.](image)

Similarly to the L-TLM, the bias is applied between the circular and the outer contacts and the current is measured. For a 200 µm diameter circular contact (used in our study) and gap spacing between 12 and 48 µm, a correction factor is necessary to compensate the difference with L-TLM. Without the correction factor, plotting the total resistance $R_T$ versus d leads a non-linear data, consequently, $\rho_C$ is underestimated. Fig. B-6 shows $R_T$ versus d with (black diamond) and without (red squares) the correction factor.
Fig. B-6. Total resistance as function of the distance d between the contacts before (red squares) and after (black diamond) correction.

From Fig. B-6, one can extract the sheet resistance and the transfer length. Consequently, $\rho_C$ and $R_c$ are calculated as shown in Table B-2.

**Table B-2.** Extracted and calculated electrical parameters characterizing the ohmic contact.

<table>
<thead>
<tr>
<th>Sheet resistance $R_{sh}$ ($\Omega/\square$)</th>
<th>Specific contact resistivity $\rho_C$ ($\Omega \text{ cm}^2$)</th>
<th>Transfer length $L_T$ (mm)</th>
<th>Contact resistance $R_c$ (Ω mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P \mu m \times$ slope $\left( \frac{R_C(0) \times P \text{ cm}}{2} \right)^2$</td>
<td>$\frac{10 \sqrt{\rho_C/R_{sh}}}{L_T \times R_{sh}}$</td>
<td>$L_T \times R_{sh}$</td>
<td>$L_T \times R_{sh}$</td>
</tr>
</tbody>
</table>
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Georgio EL ZAMMAR
Process of high power Schottky diodes on the AlGaN/GaN heterostructure epitaxied on Si

Résumé
Les convertisseurs à base de Si atteignent leurs limites. Face à ces besoins, le GaN, avec sa vitesse de saturation des électrons et le champ électrique de claquage élevés est candidat idéal pour réaliser des redresseurs, surtout s’il est épitaxié sur substrat à bas cout. Ce travail est dédié au développement des diodes Schottky sur AlGaN/GaN. Une couche de SiNx en faible traction a été obtenue. Un contact ohmique de Ti/Al avec une gravure partiel a donné une Rc de 2.8 Ω:mm avec une résistance Rsh de 480 Ω/□. Des diodes Schottky avec les étapes issues de ces études ont été fabriqué. La diode recuite à 400 ºC avec 30 nm de profondeur de gravure a montré une hauteur de barrière de 0.89 eV et un facteur d’idéalité de 1.49. La diode a présenté une très faible densité de courant de fuite de 8.45x10^{-8} A.mm^{-1} à -400 V avec une tension de claquage entre 480 V et 760 V.

Mots clés : grand gap, GaN, passivation, contact ohmique, contact Schottky, implantation ionique, caractérisation électrique.

Abstract
Si-based devices for power conversion applications are reaching their limits. Wide band gap GaN is particularly interesting due to the high electron saturation velocity and high breakdown electric field, especially when epitaxied on low cost substrates such as Si. This work is dedicated to the development and fabrication of the Schottky diode on AlGaN/GaN on Si. SiNx passivation in very low tensile strain is used. Ti (70 nm)/Al (180 nm) partially recessed ohmic contacts annealed at 800 ºC exhibited a 2.8 Ω:mm Rc with a sheet resistance of 480 Ω/sq. Schottky diodes with the previously cited passivation and ohmic contact are fabricated with a fully recessed Schottky contact annealed at 400 ºC. A Schottky barrier height of 0.89 eV and an ideality factor of 1.49 are obtained. These diodes also exhibited a very low leakage current density (up to -400 V) of 8.45x10^{-8} A.mm^{-1}. The breakdown voltage varied between 480 V and 760 V.

Keywords: wide band gap, GaN, passivation, ohmic contact, Schottky contact, ion implantation, electrical characterization.